asQED Symposium 2012

SPANSION

Recent Development and Progress in Nonvolatile Memory for Embedded Market

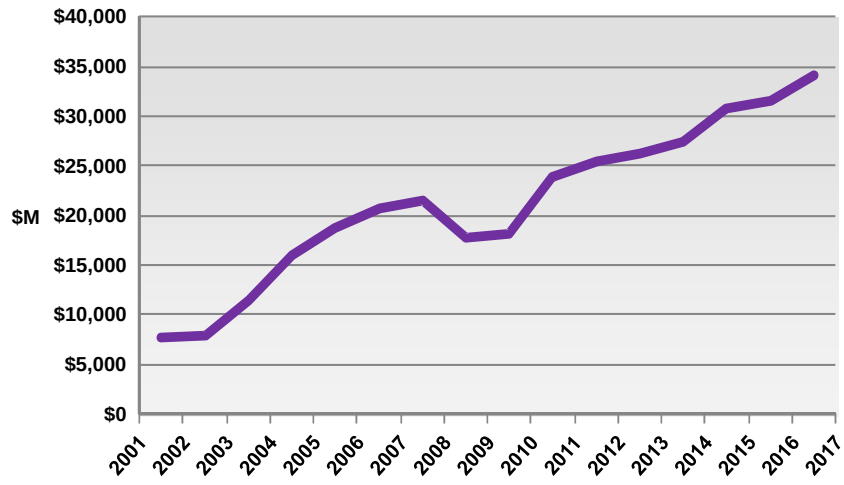
Saied Tehrani, Ph.D.
Chief Technology Officer, Spansion Inc.

July 11, 2012

Outline

- **Market Trend for Nonvolatile Memory**
- **NOR Flash**
  - Standalone
  - Embedded in SOC
- **NAND Flash**
  - Status and Market Needs
  - NAND Scaling Challenges
  - Lithography Gaps
- **Other Nonvolatile Technologies**
  - Phase Change Memory
  - Resistive RAM
  - MRAM
- **Summary**

Total Flash Market



Source: iSupply

SPANSION

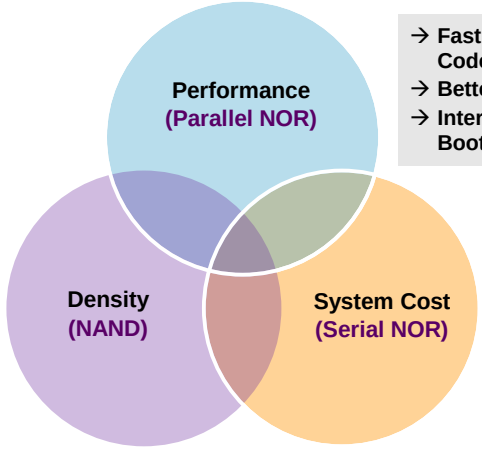
Enabling Innovation

SPANSION

Enabling Disruption

SPANSION

Flash Memory for Every Design Need



→ Fast Read for Fast Code / Data Access
→ Better Reliability
→ Interactivity and Boot Times

→ High Density / Low Cost
→ Compromised Reliability
→ Data Storage

→ Low Density / Fewer Pins
→ Better Reliability
→ Serial Slow Access
→ Code Boot

SPANSION

NOR and NAND Flash for Embedded Market

Auto Infotainment

- Multi-language interfaces, rich graphics, user configuration data
- Parallel NOR for fast boot
- Embedded SLC NAND data storage

Set-top Box / TV

- Internet and app support drives larger software requirements
- Serial NOR for fast boot
- Embedded SLC NAND for reliable application storage

Communications

- Multi-mode base stations drive increased software complexity
- Parallel NOR for fast boot
- Embedded SLC NAND data storage

Outline

Market Trend for Nonvolatile Memory

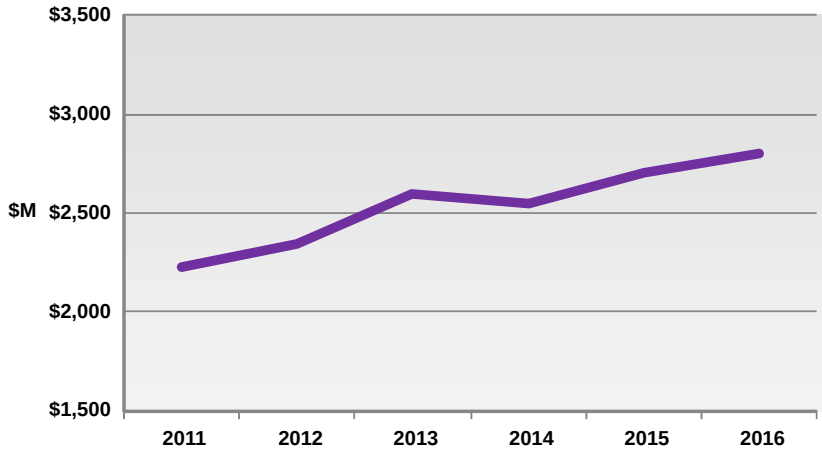
NOR Flash
- Standalone
- Embedded in SOC

NAND Flash
- Status and Market Needs
- NAND Scaling Challenges
- Lithography Gaps

Other Nonvolatile Technologies
- Phase Change Memory
- Resistive RAM
- MRAM

Summary

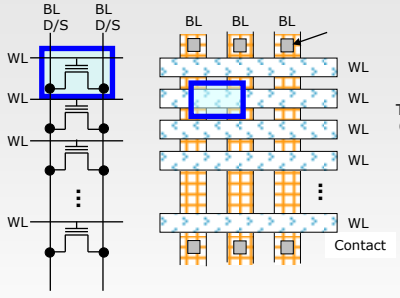
Embedded NOR Flash TAM

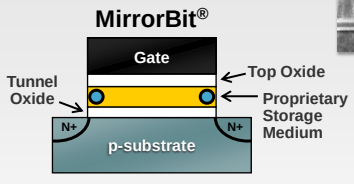


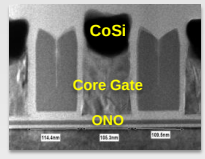
Source: iSupply

SPANSION

NOR Flash Memory Cell – MirrorBit® Technology



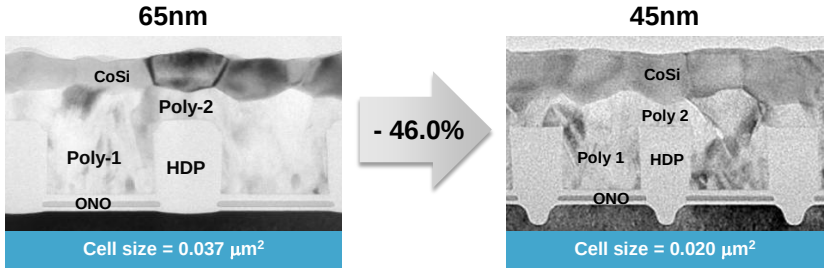




- MirrorBit cell stores charge in two physically different locations
- Non-conducting storage dielectric
  - Doubles device density
- Symmetric transistor
  - Selectable source-drain
  - Simple, planar structure

SPANSION

Spansion 45nm Technology

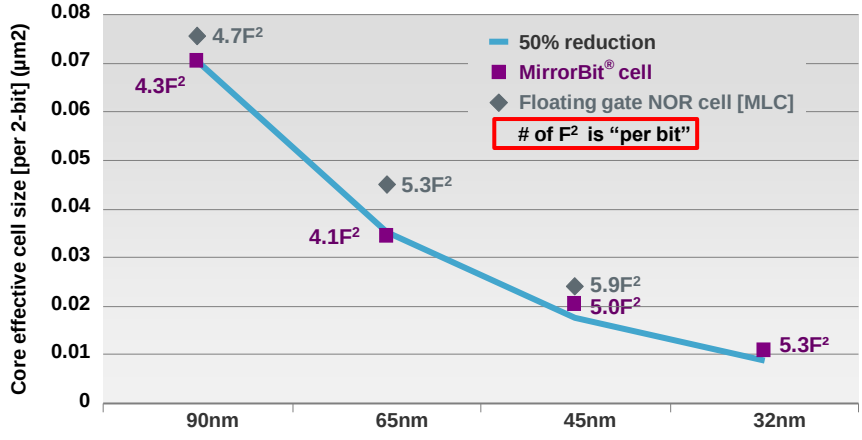


45nm Technology

- Junction engineering to optimize doping profile
- Bit line trench to minimize neighboring bit program disturb
- Optimized program and erase algorithms
- Performance and reliability same as 65nm

SPANSION

NOR Cell Size Scaling Example



Spansion Product Introduction	In Production	2012	2015

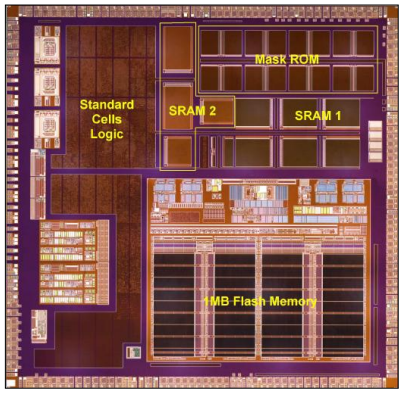
Source: Spansion estimates

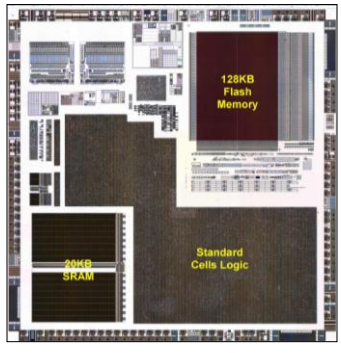
SPANSION

Outline

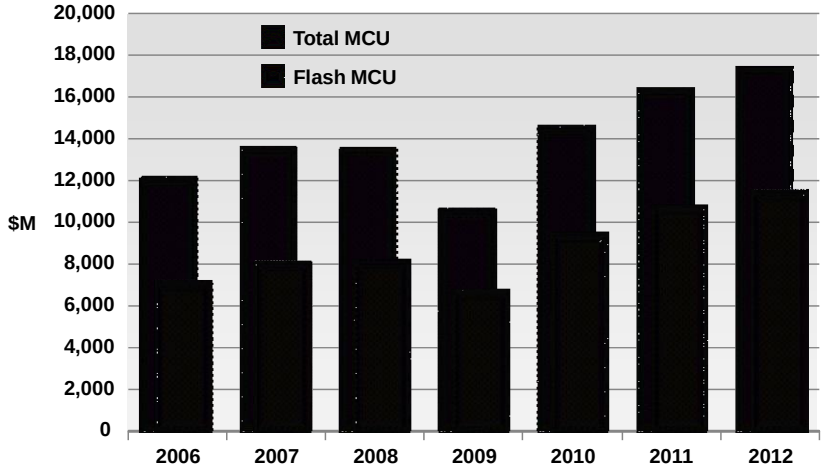
- **Market Trend for Nonvolatile Memory**
- **NOR Flash**
  - Standalone
  - Embedded in SOC
- **NAND Flash**
  - Status and Market Needs
  - NAND Scaling Challenges
  - Lithography Gaps
- **Other Nonvolatile Technologies**
  - Resistive RAM
  - Phase Change Memory
  - MRAM
- **Summary**

Embedded Flash in Microcontrollers (MCU)





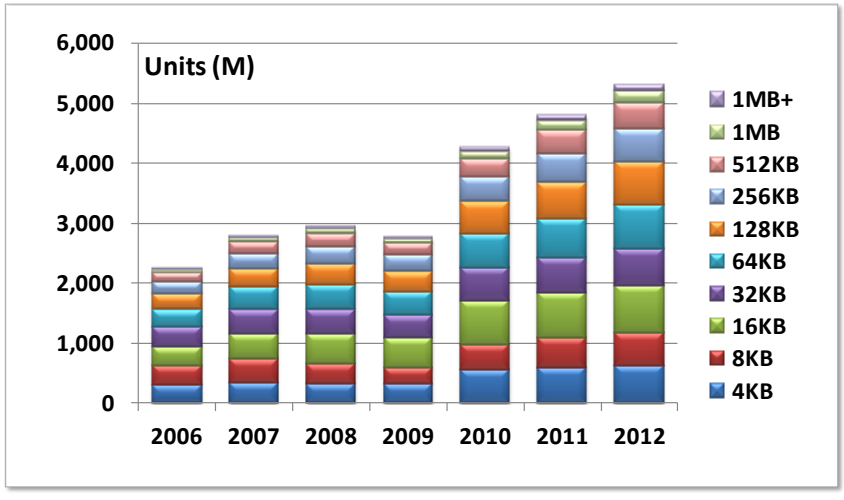
MCU TAM



Source: Semico

SPANSION

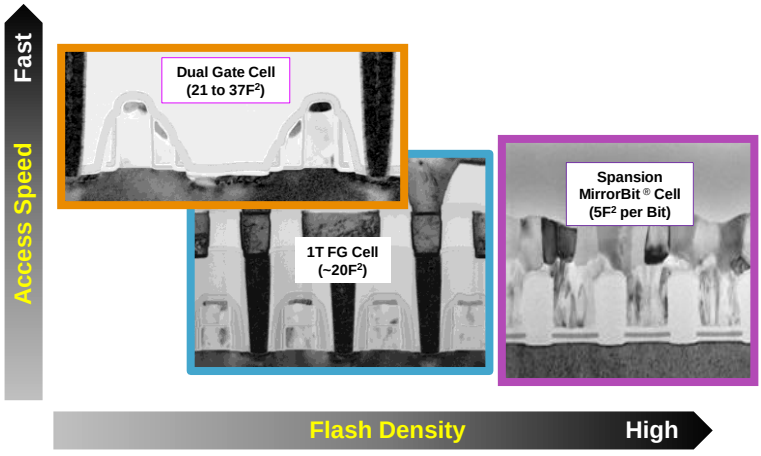
MCU Volume by Embedded Flash Density



Source: Semico

SPANSION

Embedded NOR Flash



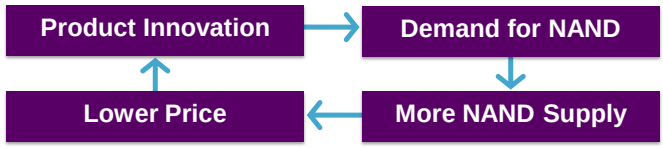
SPANSION

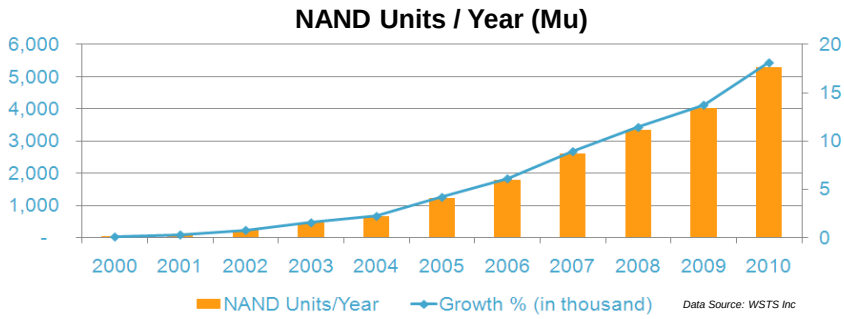
Outline

- **Market Trend for Nonvolatile Memory**
- **NOR Flash**
  - Standalone
  - Embedded in SOC
- **NAND Flash**
  - Status and Market Needs
  - NAND Scaling Challenges
  - Lithography Gaps
- **Other Nonvolatile Technologies**
  - Phase Change Memory
  - Resistive RAM
  - MRAM
- **Summary**

SPANSION

Rapid NAND Growth Cycle

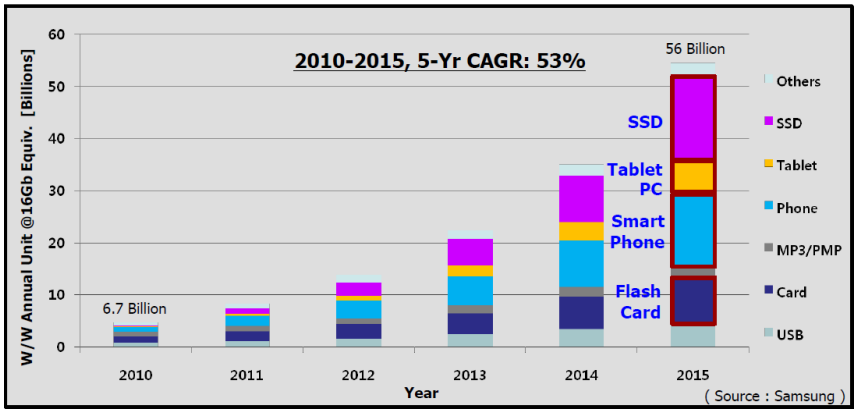




NAND Industry Experienced 18,000% Volume Growth in 10 Years

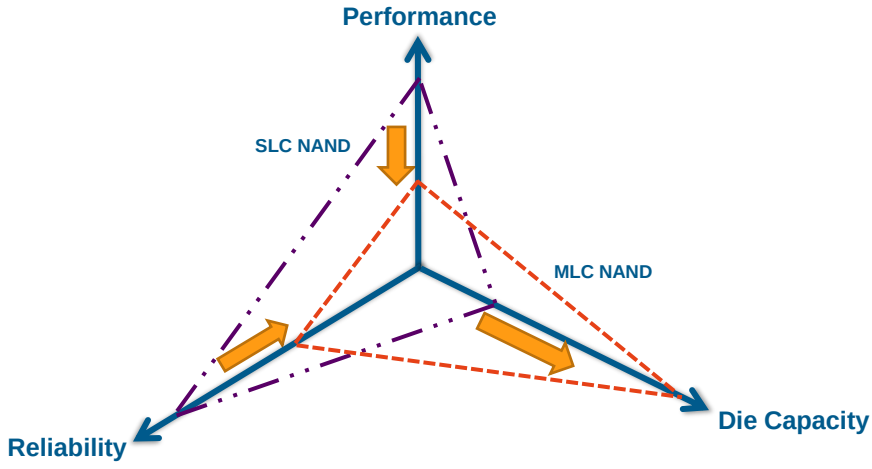
SPANSION

NAND Flash Market Outlook



SPANSION

Higher Density at the Cost of Performance and Reliability

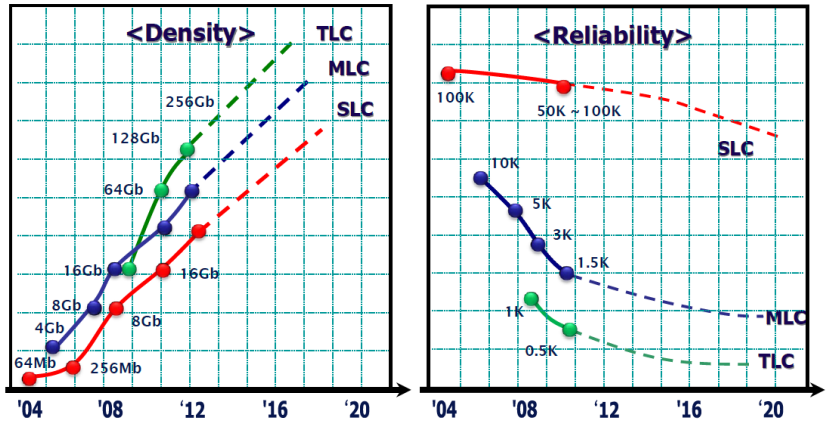


- From SLC NAND to MLC and TLC NAND
- Process technology shrink every 18 months

SPANSION

NAND Technology Migration

Density has doubled every year since 2004



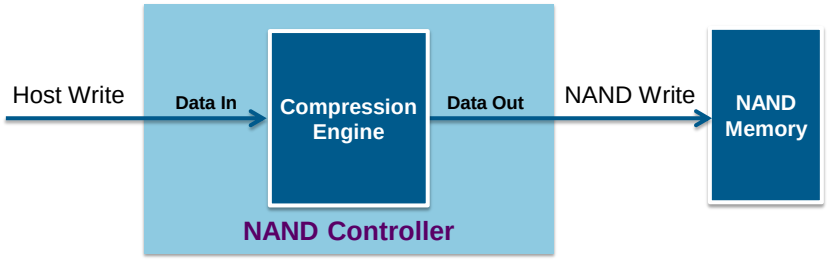
Source: Samsung

SPANSION

Managing Around Lower Quality NAND

- Write Amplification = NAND Write / Host Write
- Lower Write Amplification
  → Less Writes to the NAND
  → Extended NAND life
- Efficient controllers are implementing firmware with lower Write Amplification to extend life of NAND

Improving Performance and Quality



Size of Data Out << Size of Data In

- **Data Compression** reduces amount of data written to the NAND
  - Less data Writes increases performance
  - Less data Writes increases NAND life
- **Wear Leveling** is another mechanism to improve application quality
  - NAND Data is moved from one physical location to another periodically to balance the wear-out of NAND cells

Outline

Market Trend for Nonvolatile Memory

NOR Flash
- Standalone
- Embedded in SOC

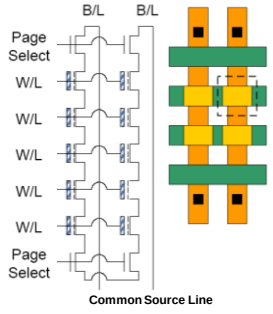
NAND Flash
- Status and Market Needs
- NAND Scaling Challenges
- Lithography Gaps

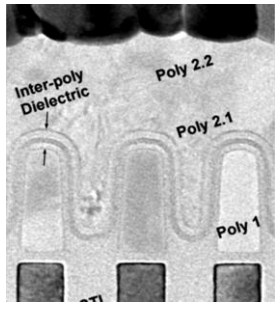
Other Nonvolatile Technologies
- Phase Change Memory
- Resistive RAM
- MRAM

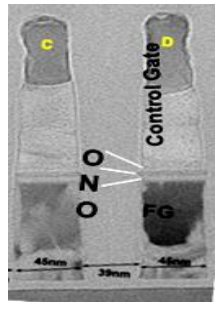
Summary

NAND Cell and Architecture

Array Interconnections

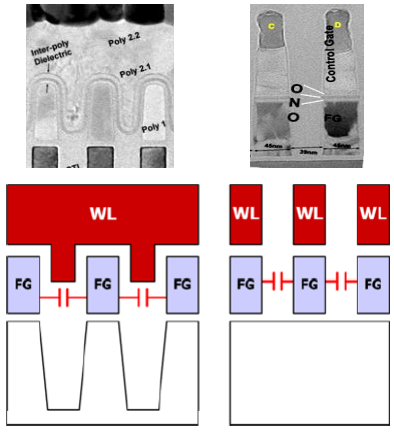




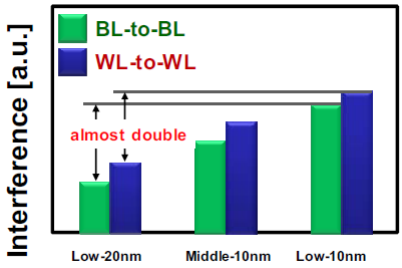


Cell Size ~ $4.0F^2$

Scaling Challenges in NAND: Interference



Capacitive coupling between neighboring Word and Bit lines

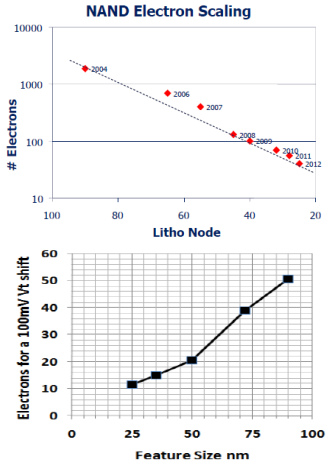


Simulation results show WL-to-WL and BL-to-BL interferences double going from low-20nm to low-10nm node

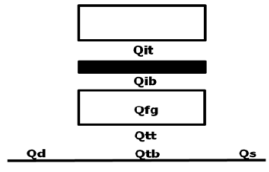
Seokkiu Lee, Memory Workshop (IMW), pp.6-9, 2012

SPANSION

Scaling Challenges in NAND: Fewer Electrons and Larger Variation



Number of electrons required for 100mV Vt shift vs. cell feature size.



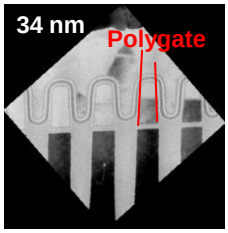
	50nm	35nm	25nm
Qtb	4	2	1
Qtt	9	7	4
Qib	22	17	9
Qit	149	103	100
Qs	33	9	5
Qd	61	16	10
Qfg	18	12	10

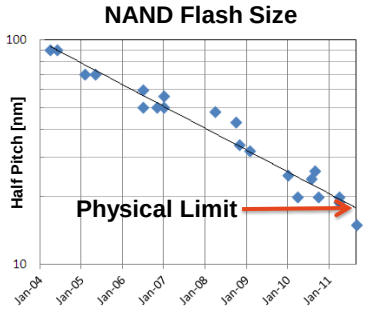
Location of parasitic charge in a NAND cell and the required number of electron at these locations to shift the cell Vt by 100mV

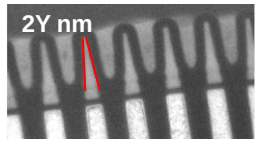
Kirk Prall and Krishna Parat, IEDM 2010, pp. 102-105

SPANSION

Floating-Gate NAND Scaling Limitation



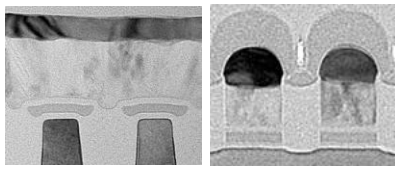




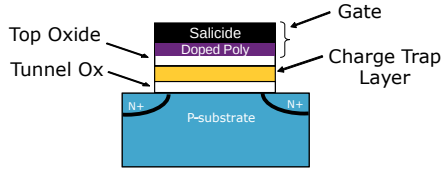
Below 20nm — **The conventional ONO interlayer poly dielectric does not fit the pitch**

SPANSION

Alternative NAND Architecture: Planar Charge Trap NAND



Cell Size $4.0F^2$

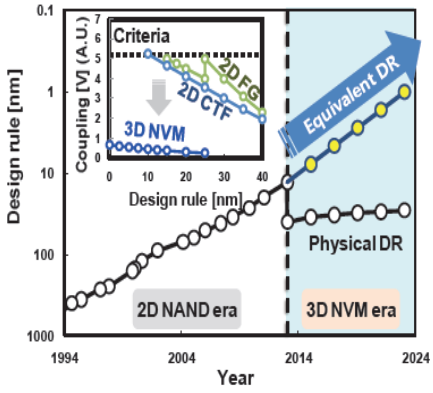


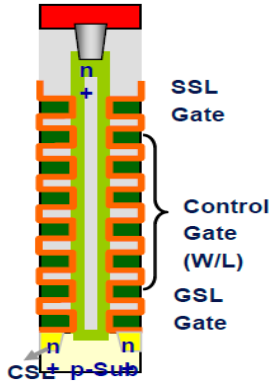
Charge Trap Storage Device

- **Charge Trap cell in standard NAND array architecture**
- **Planar architecture**
- **Reduced interference coupling of neighboring cell**

SPANSION

Alternative NAND Architecture: 3D





Jungdal Choi and Kwang Soo Seol, VLSI Tech. Digest, 178-179, 2011

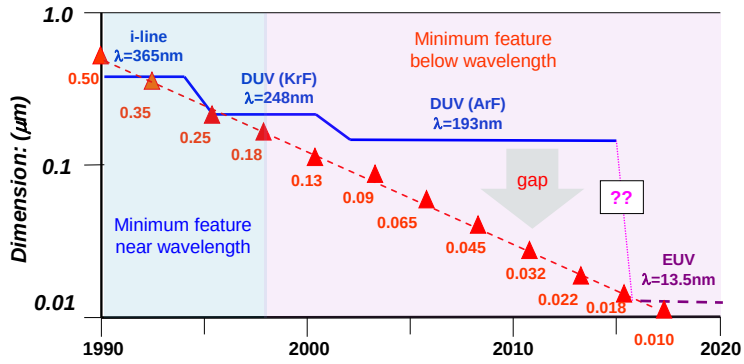
SPANSION

Outline

- **Market Trend for Nonvolatile Memory**
- **NOR Flash**
  - Standalone
  - Embedded in SOC
- **NAND Flash**
  - Status and Market Needs
  - NAND Scaling Challenges
  - Lithography Gaps
- **Other Nonvolatile Technologies**
  - Phase Change Memory
  - Resistive RAM
  - MRAM
- **Summary**

SPANSION

Lithography Roadmap



Serge Tedesco, CEA LETI. 2012 NIKON Litho Vision Presentation

Rayleigh's Formula:

$$pitch = \frac{\lambda}{(1+\sigma)\cdot NA}$$

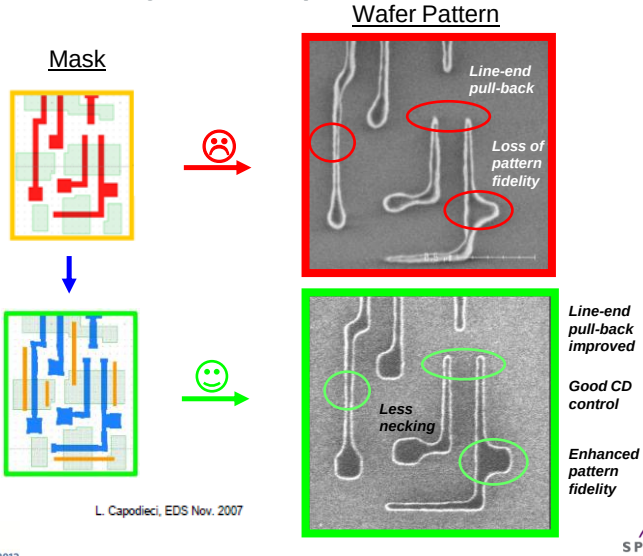
$$Min.\ feature = k_1 \cdot \frac{\lambda}{NA}$$

- **Smaller wavelength and larger NA achieve finer pitch**
  - **Maximum NA of 1.35 for 193 nm Immersion**
- **Challenge is to maintain high k1 for manufacturability while reducing min. feature**

SPANSION

Technique to Extend Litho Tool Capability (A)

RET (Resolution Enhancement Technology) by OPC (Optical Proximity Correction)



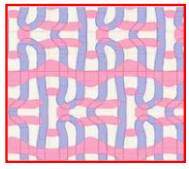
L. Capodieci, EDS Nov. 2007

SPANSION

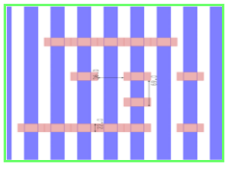
Technique to Extend Litho Tool Capability (B)

DFM (Design for Manufacturability): Changing cell layout to improve lithography performance

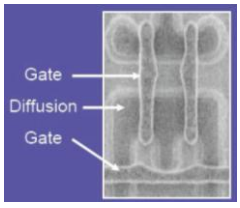
Irregular active and gate patterns



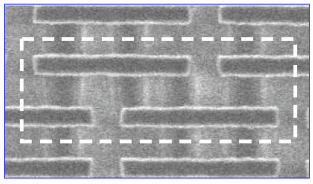
Vertical pattern for active
Horizontal pattern for gate



Difficult to print – requires intensive OPC



Easy to print



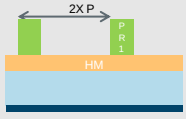
Yan Borodovsky, Intel. 2006 SPIE Microlithography, San Jose, CA

SPANSION

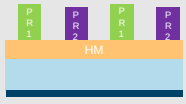
Technique to Extend Litho Tool Capability (C)

Double (or Quadruple) Patterning to extend process window by relaxing pitch to achieve fine patterns

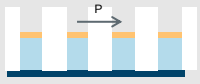
Example 1 (Litho-Litho-Etch)



1) Print the1st pattern with 2X pitch

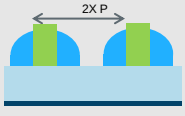


2) Coat and print the 2nd pattern between the formed 1st pattern



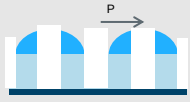
3) Transfer the lithography pattern to the hardmask and substrate

Example 2 (Self-Aligned Double Patterning)



1) Print and form the 1st pattern with 2X pitch

2) Film deposition and etch to form the spacer as hardmask



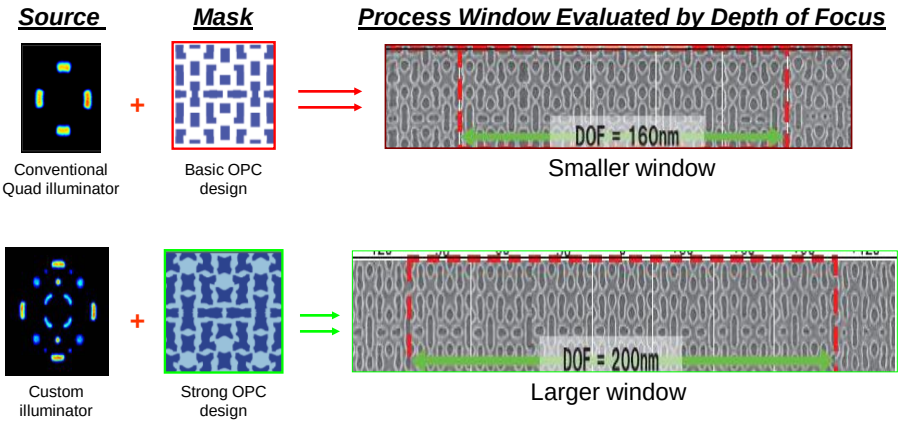
3) Transfer the spacer to the substrate layer

Quadruple patterning can further achieve 2x more pattern density

SPANSION

Technique to Extend Litho Tool Capability (D)

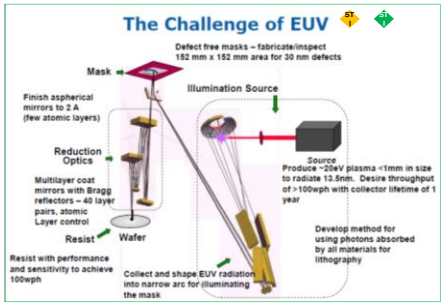
SMO (Source-Mask Optimization) to extend process window by optimizing illuminator and OPC based on layout pattern



Naoya Hayashi, DNP, 2012 NIKON Litho Vision Presentation

SPANSION

Next Generation Lithography Tool: EUV

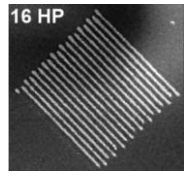


		Half-Pitch Size (nm)						
		20	18	16	14	13	11	9
EUV Wavelength	System NA	K1 factors for EUVL						
13.5 nm	0.25	0.37	0.33	0.30	0.26	0.24	0.20	0.17
	0.33	0.49	0.44	0.39	0.34	0.32	0.27	0.22
	0.35	0.52	0.47	0.41	0.36	0.34	0.29	0.23
	0.40	0.59	0.53	0.47	0.41	0.39	0.33	0.27
	0.45	0.67	0.60	0.53	0.47	0.43	0.37	0.30
	0.50	0.74	0.67	0.59	0.52	0.48	0.41	0.33
6.7nm	0.20	0.60	0.54	0.48	0.42	0.39	0.33	0.27
	0.30	0.90	0.81	0.72	0.63	0.58	0.49	0.40
	0.40	1.19	1.07	0.96	0.84	0.78	0.66	0.54

Technical Challenges

- **EUV source intensity –** Low wafer throughput
- **Mask inspection –** Embedded defect in the blank
- **Mirror reflectivity / contamination –** Cleaning frequency / downtime
- **Resist maturity –** Still in development

16nm half-pitch EUV resist lines



J.K. Stowers et. al., Proc. of SPIE Vol. 7969, 2011

More advanced EUV system under development to achieve < 10nm half-pitch

Katsuhiko Murakami, NIKON, From 2012 NIKON Litho Vision Presentation

SPANSION

Lithography Trend

- ArF (193nm) lithography already extended to 1X nm node
  - More innovative approaches under development to further extend ArF capability
- EUV lithography significantly improved
  - Need to resolve manufacturing challenges
  - Target technology: 16nm node or smaller

Outline

Market Trend for Nonvolatile Memory

NOR Flash
- Standalone
- Embedded in SOC

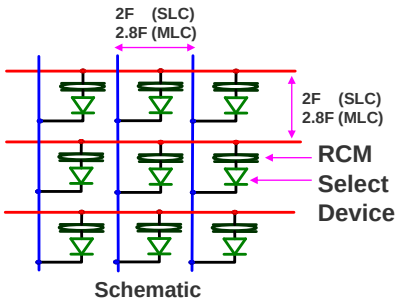
NAND Flash
- Status and Market Needs
- NAND Scaling Challenges
- Lithography Gaps

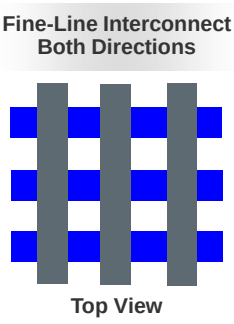
Other Nonvolatile Technologies
- Phase Change Memory
- Resistive RAM
- MRAM

Summary

Resistive Change Memory Building Blocks

Three Critical Components





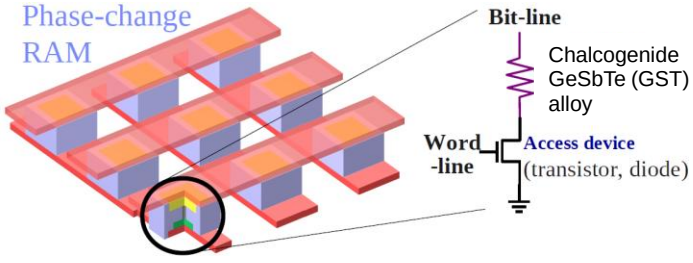
Resistive Change Element

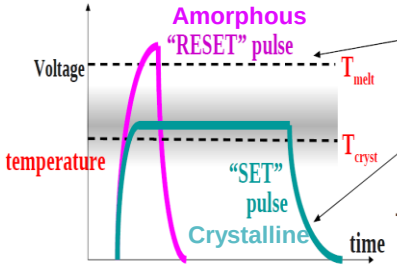
Phase-Change Memory
or
Resistive RAM

~4F² RCM components:
1. MLC RCM memory device
2. Compact select device
3. Fine-line interconnect

SPANSION

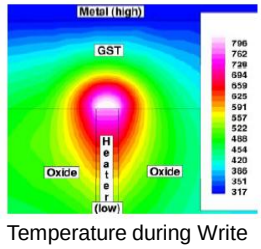
Phase-Change RAM





High current:
Scaling

Set pulse time:
Performance

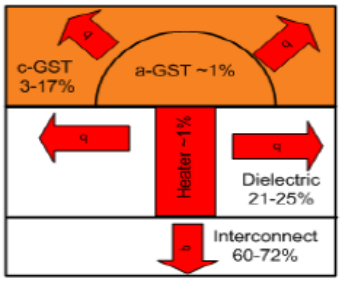


Temperature during Write

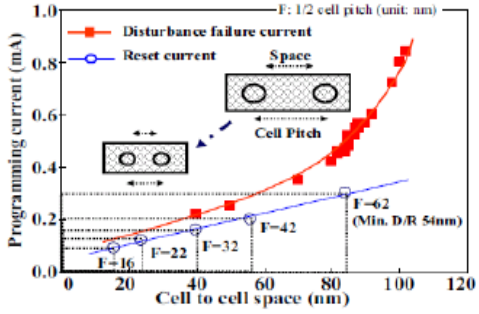
Source: Micron

SPANSION

Phase Change Memory Scaling Challenges



Heat Loss
from a PCM cell [1,2]

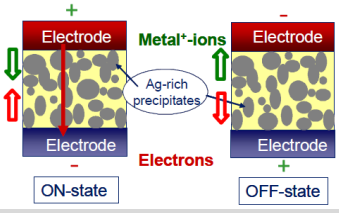


Loss of margin between set and reset current with scaling [3]

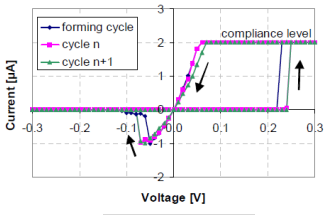
[1] S. Sadeghipour, ITHERM, 2006
[2] J. Tominga, et al., EPCOS, 2010
[3] S. Raox, et al, Phase Change Materials Science and Application, Spring 2009.

SPANSION

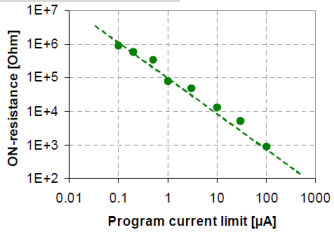
Conductive Bridge RAM (CBRAM)



Schematic illustration of the CBRAM conduction mechanism



DC switching

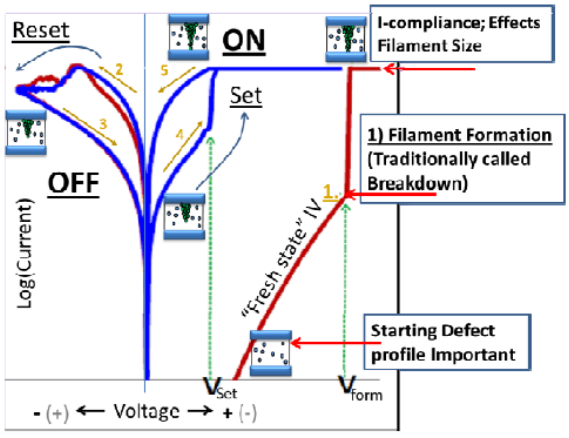


ON- state resistance dependence on programming current

Micheal Kund, et al., IEDM, 2005 & NVMTS, 07

SPANSION

Oxygen Vacancy Based RRAM

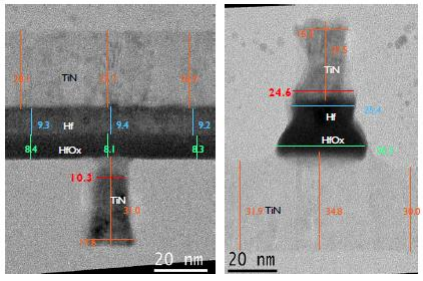


DC bi-polar switching characteristics. Oxygen vacancies convert the dielectric into a metal-rich filament (ON state) and reset (off state) by oxidation of the narrower tip of the conductive filament.

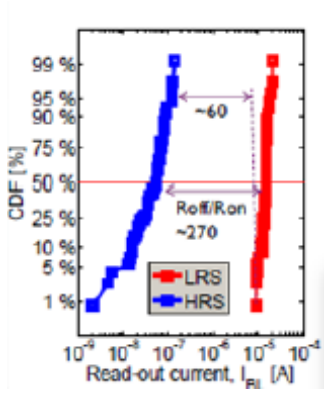
D. C, Gilmer, IMW, IEDM, 2012

SPANSION

Oxygen Vacancy-based Resistive RAM



Memory Stack:
TiN/10nm HfO2/10nm Hf/TiN

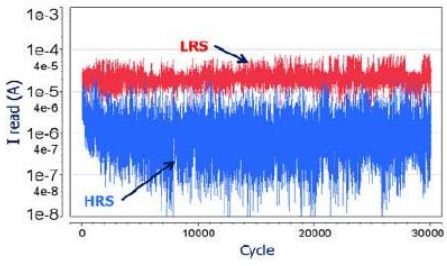


Distribution for ON/OFF states with adaptive switching

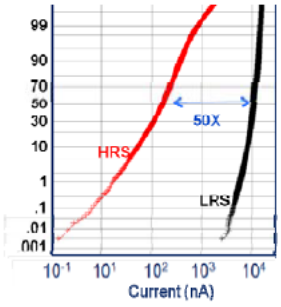
B. Govoreanu, et el, IEDM, 2011

SPANSION

Issues with O-RRAM



Significant variability in the placement of HRS and LRS with cycling



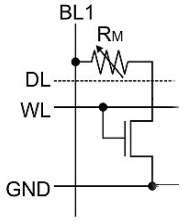
Set/Rset distributions from a 1IT1R 1M O-RRAM (no window)

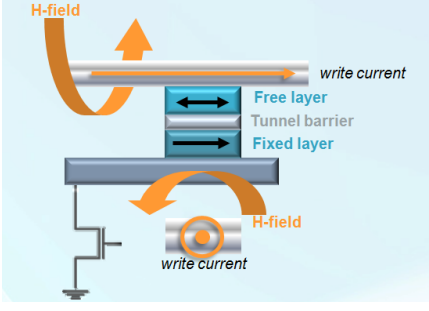
Kirk Prall, et al., Memory Workshop (IMW), pg. 1-5, 2012

SPANSION

In Production: Toggle MRAM

- Magnetic thin film as a storage element
- SRAM random access speed-35nm Read & Write Cycle time
- Magnetic Polarization rather than charge storage
- Densities of 256kb-16Mb in production (180nm-130nm)
- Challenging to scale to small geometries & reduce write current



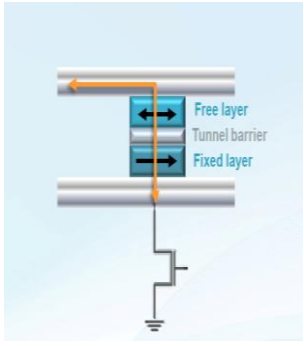


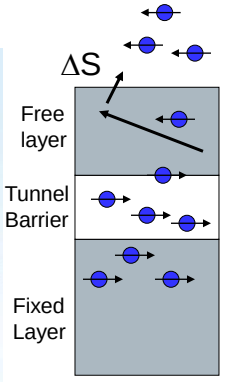
Source: Everspin

SPANSION

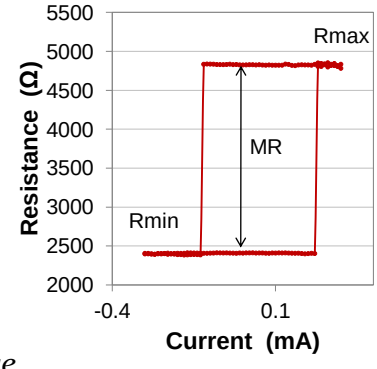
In Development: Spin Torque MRAM

Use spin momentum from current to change direction of *S*, *m*.





$$\frac{\Delta S}{\Delta t} = Torque$$



Challenges: Achieving low program current, high tunnel oxide breakdown, and data retention simultaneously

Source: Everspin

SPANSION

Summary

- Nonvolatile memory market continues to grow with evolution of smarter and lighter portable products
- Flash memory is now leading the semiconductor industry in requiring the most advanced lithography technologies
- NOR and NAND Flash provide different value to the systems and will continue to coexist
- Active research in alternative Nonvolatile memories to address performance or scalability challenges of traditional Nonvolatile memory technologies

SPANSION