August 27, 2013
Penang, Malaysia

A Possibility of Crystalline Indium-Gallium-Zinc-Oxide

asQED symposium 2013

(5th Asia Symposium on Quality Electronic Design)

Shunpei Yamazaki
Semiconductor Energy Laboratory Co.,LTD.,
398 Hase, Atsugi-shi, Kanagawa, Japan

SEL
SEMICONDUCTOR ENERGY LABORATORY

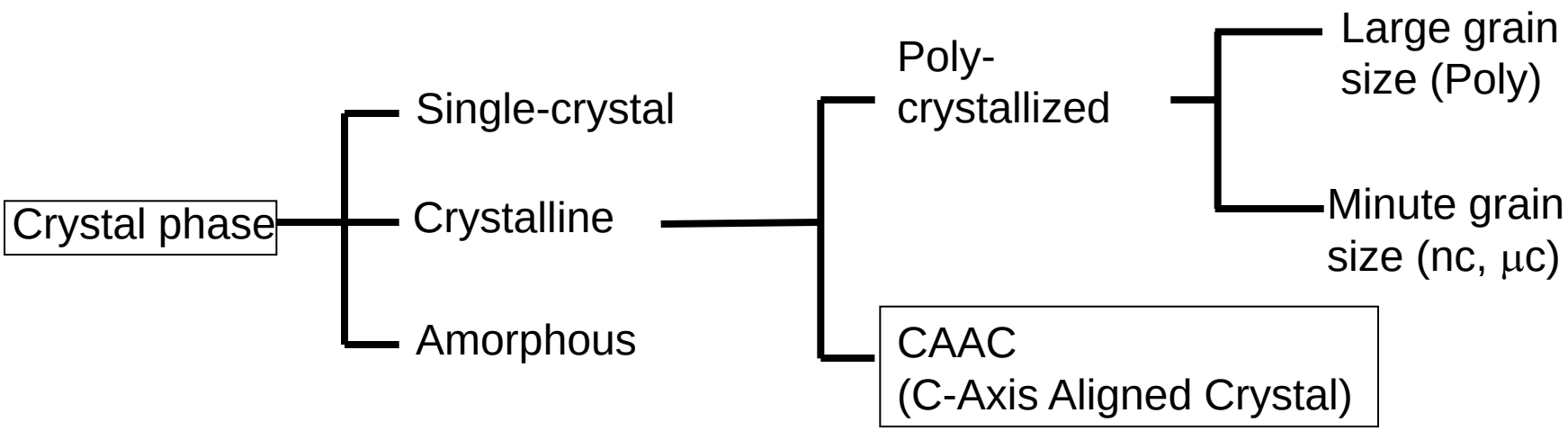
Table of Contents

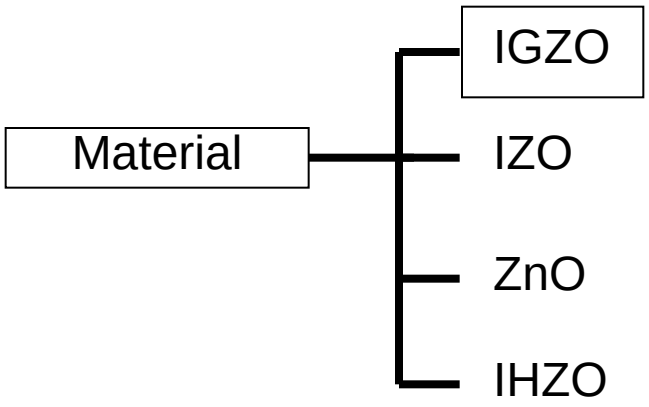
[1] Overview

1. N. Kimizuka and T. Mohri, *J. Solid State Chem.*, **60**, 382 (1985).
2. N. Kimizuka, M. Isobe, and M. Nakamura, *J. Solid State Chem.*, **116**, 170 (1995).
3. C. Chen, K-C. Cheng, E. Chagarov, and J. Kanicki, *Jpn. J. Appl. Phys.*, **50**, 091102(2011).
4. S.Yamazaki, presented at *International Workshop "Private Sector - Academia Interaction"* , organized with KVA (2011).

   http://www.icsu.org/events/ICSU%20Events/international-workshop-private-sector-academia-interaction
5. S. Yamazaki, J. Koyama, Y. Yamamoto, and K. Okamoto, *SID Symposium Digest*, **43**, 183 (2012).
6. H. Inoue, T. Matsuzaki, S. Nagatsuka, Y. Okazaki, T. Sasaki, K. Noda, D. Matsubayashi, T. Ishizu, T. Onuki, A. Isobe, Y. Shionoiri, K. Kato, T. Okuda, J. Koyama, and S. Yamazaki, *IEEE J. Solid-State Circuits*, **47**, 2258 (2012).
7. J. Koezuka K. Okazaki, T. Hirohashi, M. Takahashi, S. Adachi, M Tsubuku, S. Yamazaki, Y. Kanzaki, H. Matsukizono, S. Kaneko, S. Mori, and T. Matsuo, *SID Symposium Digest,* **44**, 723 (2013) .

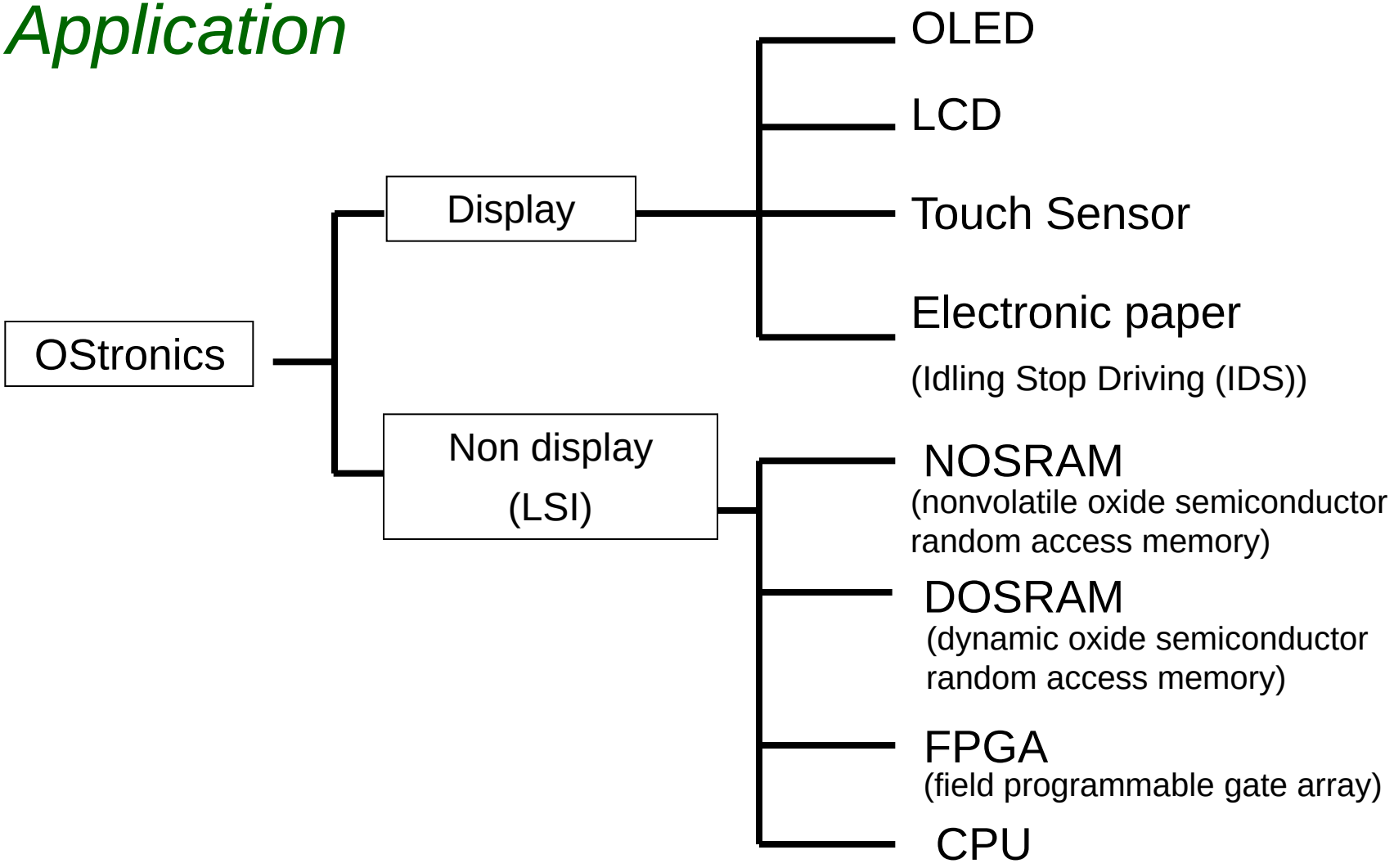
[2] Introduction





*Reference) M. Murakami *et al., Proc. AM-FPD'12* (2012).

Application



*Reference) M. Murakami *et al., Proc. AM-FPD'12* (2012).

Commercial Production of Displays Using CAAC-IGZO FET Has Begun for the First Time in the World

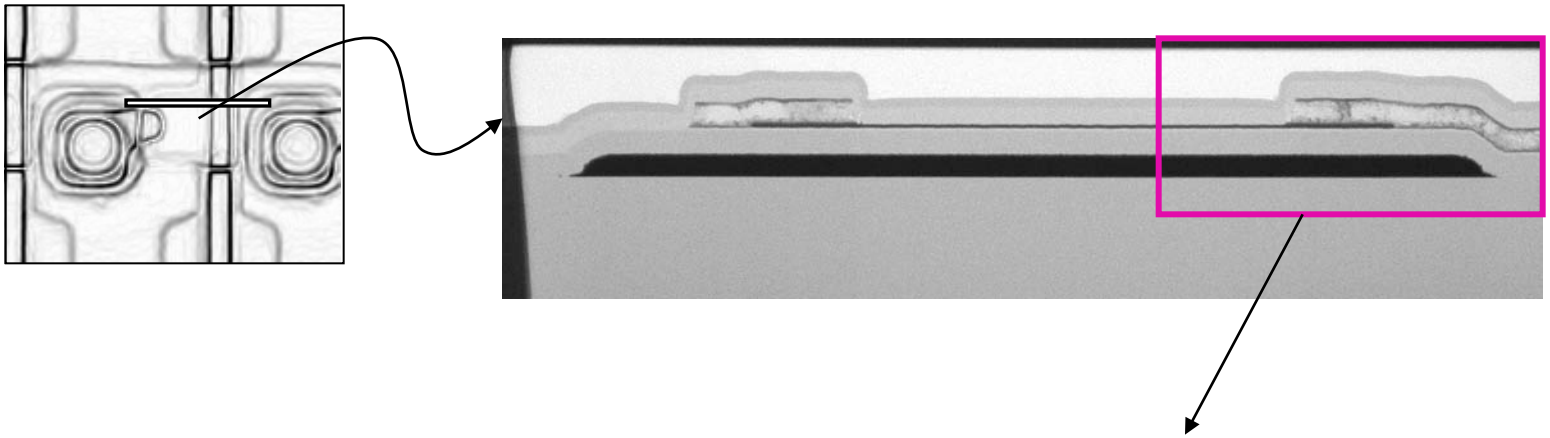
docomo NEXT series

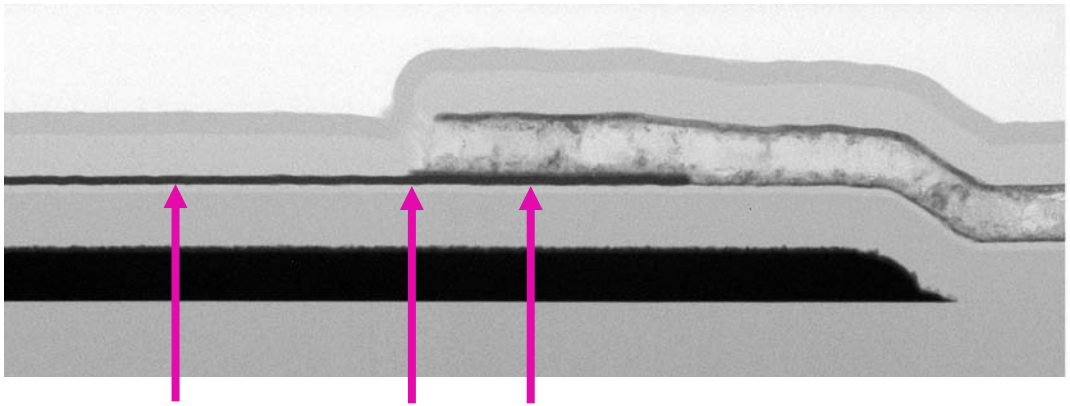
Reference: http://www.sharp.co.jp/products/sh02e/

AQUOS PHONE ZETA SH-02E

Smart phones using CAAC-IGZO FET manufactured by NTT DOCOMO, INC. and Sharp Corporation went on sale on Nov, 2012.

LCD1296 (OS)
The smart phone “AQUOS PHONE ZETA SH-02E” manufactured by Sharp, Corp.
LCD Module : 4.9 inches SHARP QM3417DP



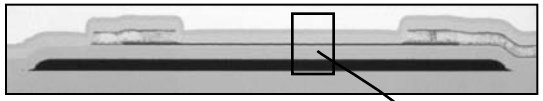


channel portion

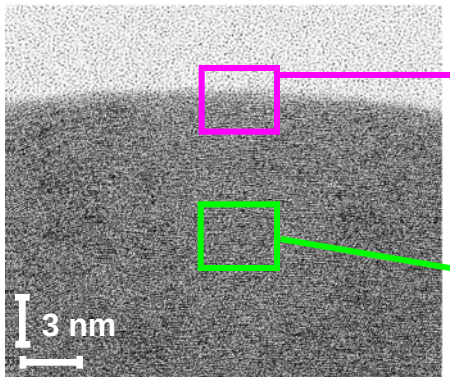
Under source-drain metal boundary

Under source-drain metal

AQUOS PHONE ZETA SH-02E
Cross-sectional TEM Image Analysis of CAAC-IGZO

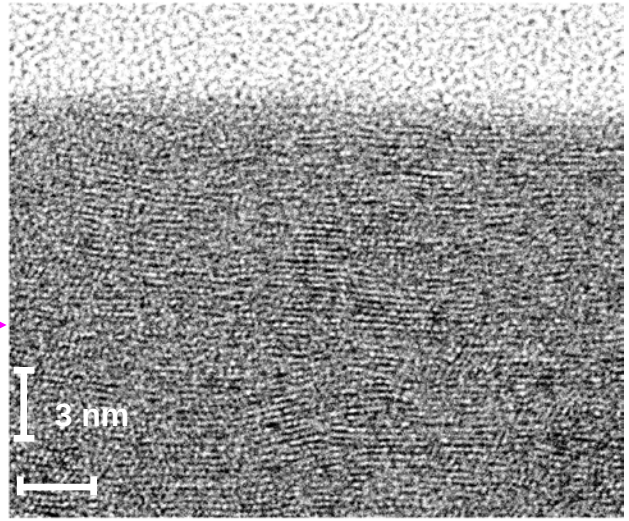


Channel portion



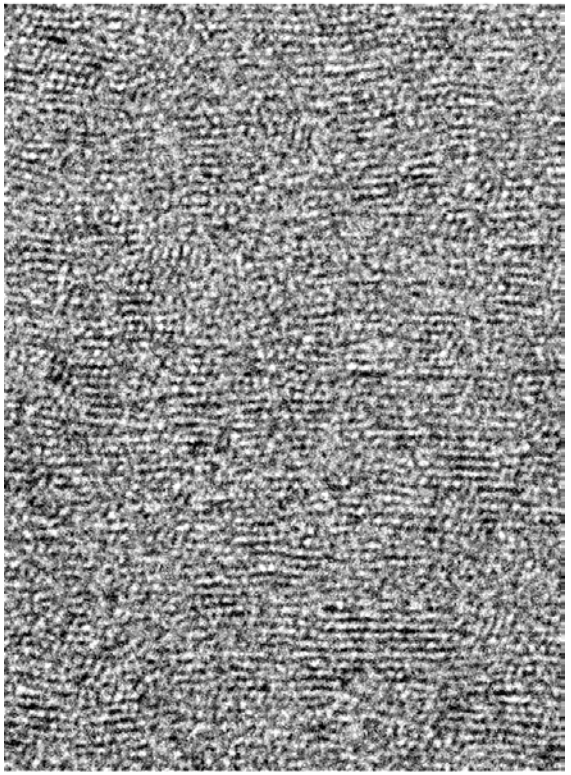
magnification : 4,000,000 times

surface of the film

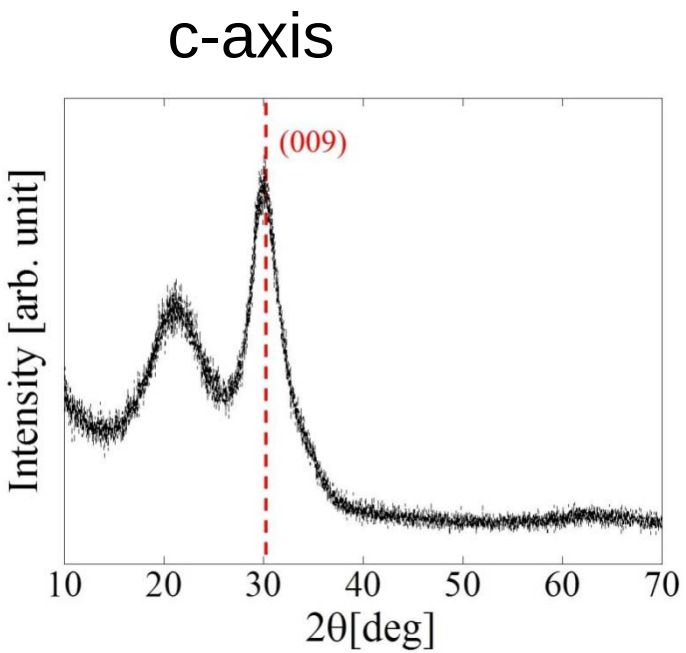


magnification : 8,000,000 times

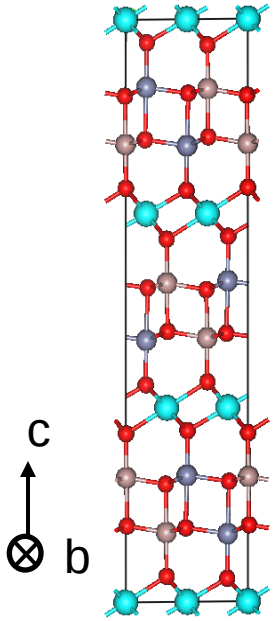
center of the film



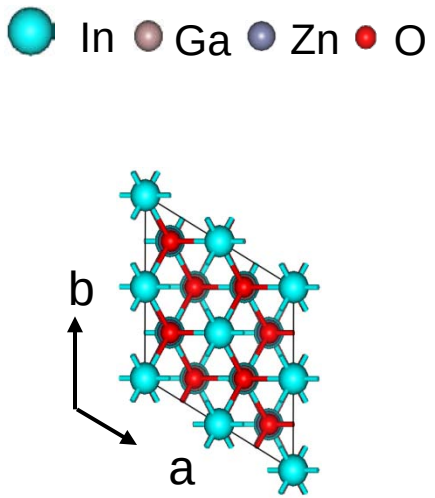
[3]What is CAAC (C-Axis Aligned Crystal)?



(a) Results of XRD Measurement of our IGZO Film



Cross sectional view



Plane view

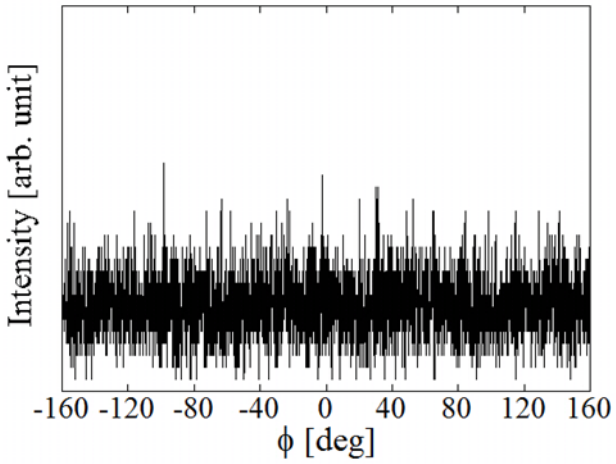
(b) Crystalline IGZO (homologous structure)

Fig. (a) shows a diffraction image of XRD (out-of-plane) on the crystalline IGZO (called CAAC hereinafter). A peak (009) is observed at around 31˚ .
Since the CAAC-IGZO has a periodic structure in Fig.(b), it has a peak in (009) in the image by XRD (out of plain).

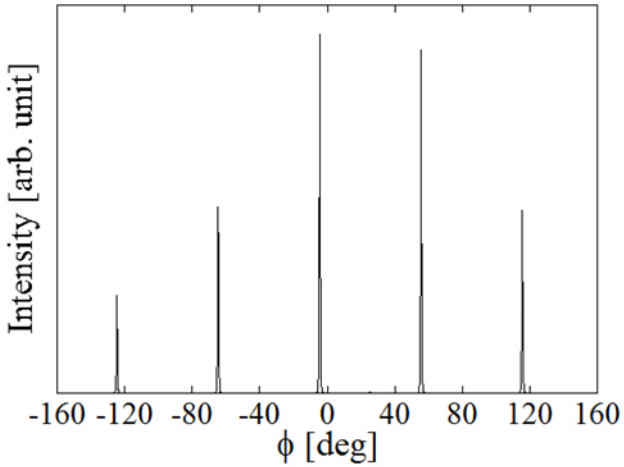
*Reference) S.Yamazaki *et al*., *SID Symposium Digest*, 43, 183 (2012).

X-Ray Diffraction (XRD) in a-b Plane

(a) CAAC-IGZO



(b) Single-Crystal IGZO



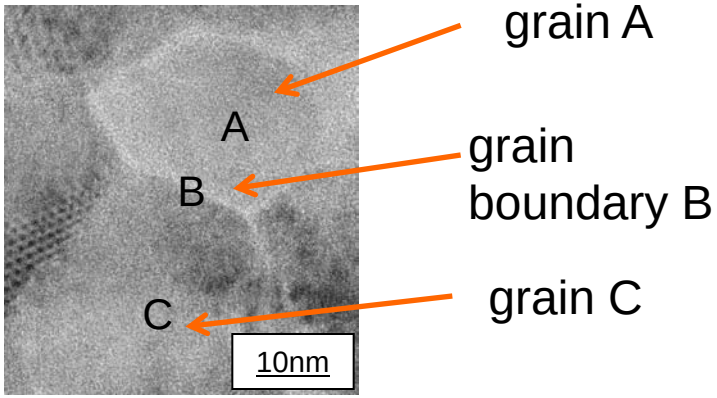
Results of In-plane XRD Measurement

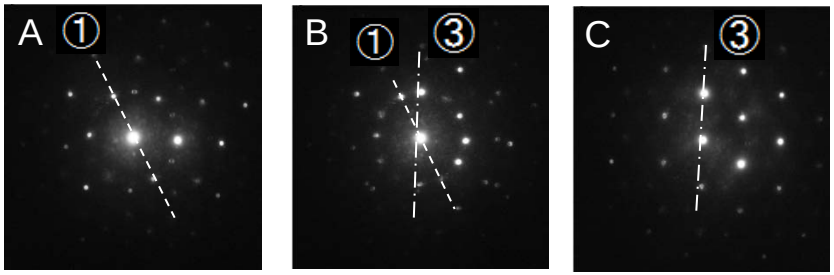
- Fig. (a) shows XRD spectra of IGZO formed over a quartz substrate with a thickness of 300 nm by an in-plane method.
- Clear diffraction peaks are observed at every 60 ° in the single-crystal IGZO having c-plane surface in Fig. (b).
- On the other hand, the CAAC-IGZO shows no diffraction peak as clear as those in the single-crystal IGZO even by rotating a sample at a 360-degree in Fig. (a), i.e. there is no symmetry in the (110) plane and no orientation in the a-b plane.

*Reference) S.Yamazaki *et al*., *SID Symposium Digest*, 43, 183 (2012).

Grain Boundary of IGZO vs. Grain region of CAAC-IGZO

(a) Laser crystallized IGZO



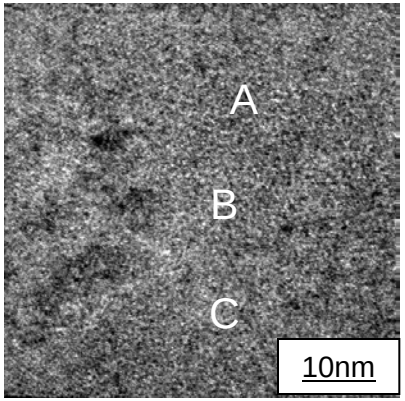


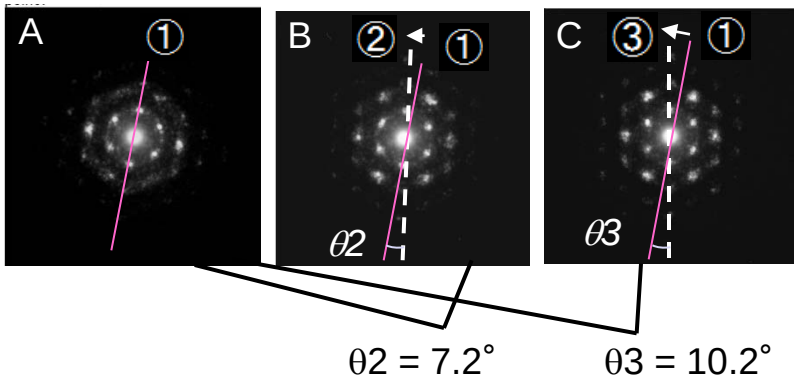
A-① and B-① have the same angle.

B-③ and C-③ have the same angle.

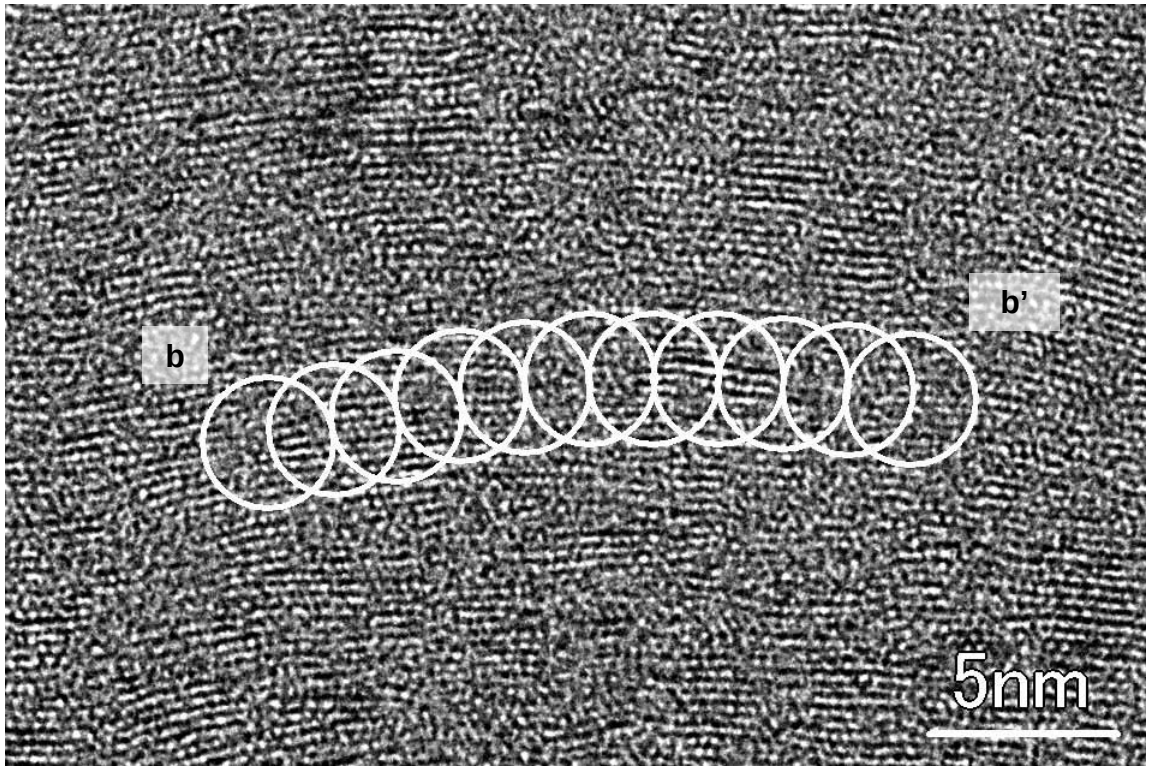
B: The same diffraction angle is observed in both A and C

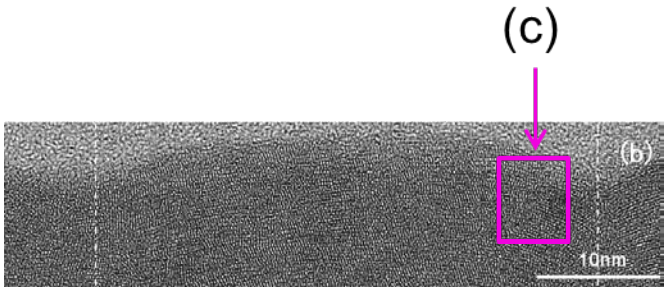
(b) CAAC (no clear grain boundary)



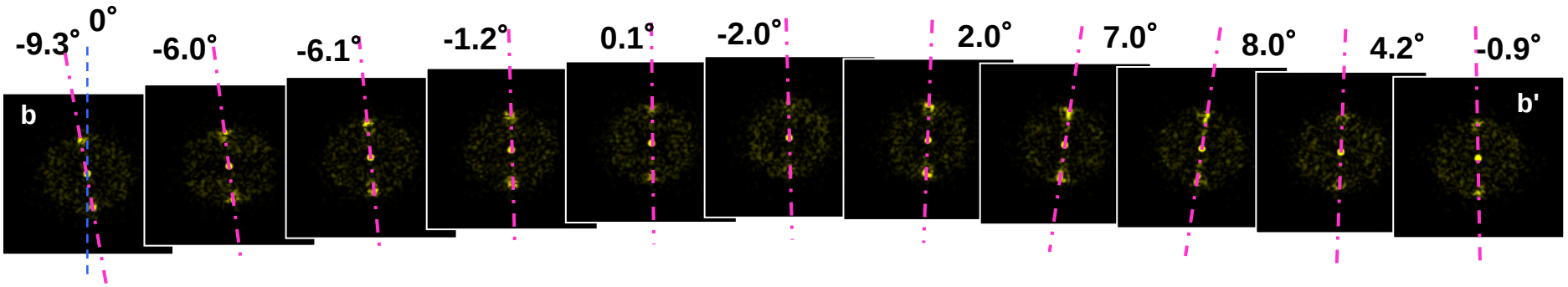


B: Observed diffraction angle rotates between and C





(c) Enlarged view of grain boundary in above image.

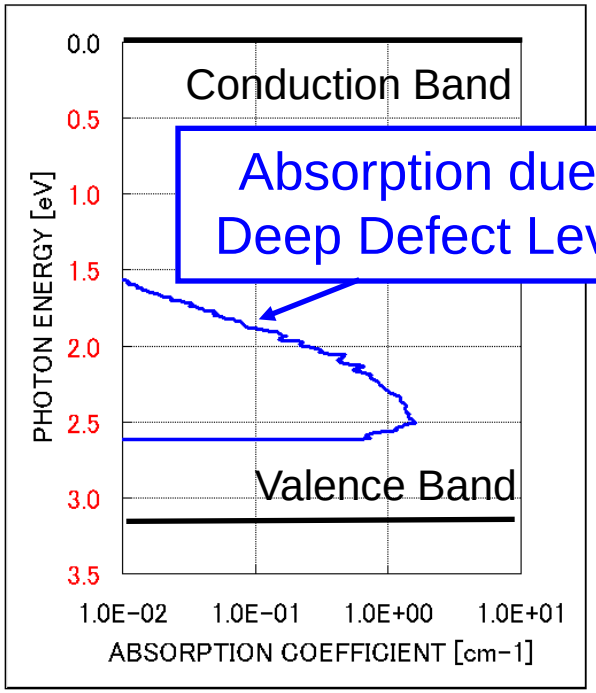


(d) Cross-sectional TEM-FFT (Fast Fourier Transform) pattern analysis of Fig. (c)

Evaluation of Deep Defect Levels in IGZO

The absorption due to deep defect levels was quantified.

Absorption due to only Deep Defect Levels



$$\alpha = \int \frac{\left(\alpha_{CPM} - \alpha_{UrbachTail}\right)}{E} dE$$

α : Absorption Coefficient of Deep Defect Levels

α_{CPM} : Absorption Coefficient Estimated by CPM

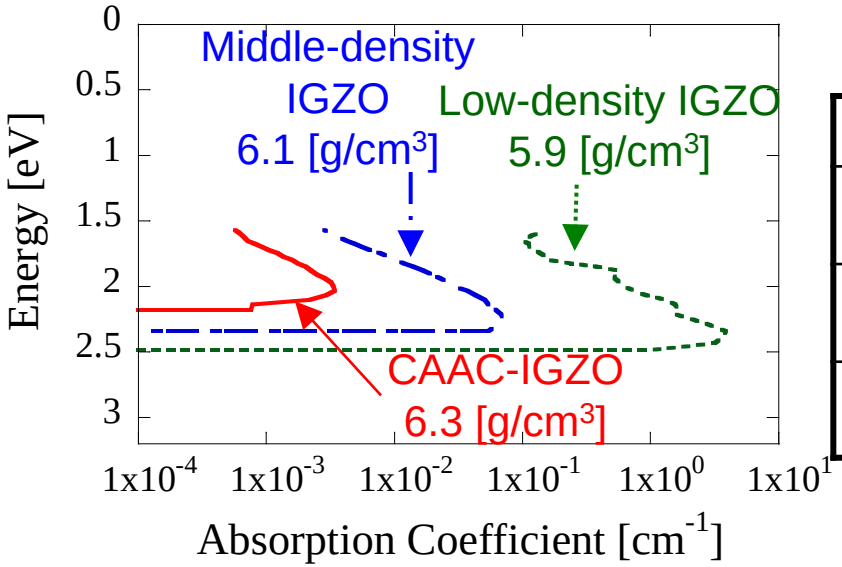
$\alpha_{Urbach\ Tail}$: Absorption due to Non-localized Levels

Quantification of Deep Defect Levels

*Reference) M.Tsubuku *et al., SID Symposium Digest*, 44, 166 (2013).

Evaluation of Deep Defect Levels in IGZO

Absorption due to deep defect levels in low-density IGZO, middle-density IGZO and CAAC-IGZO were quantified.



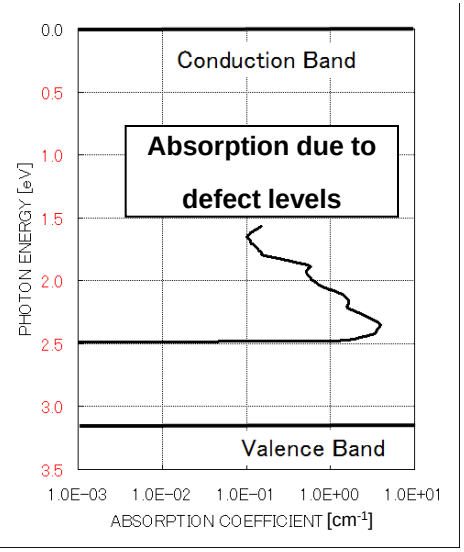
Absorption Coefficients at Sub-gap States [cm^{-1}]	
CAAC-IGZO	5.8×10^{-4}
Middle-density IGZO	1.6×10^{-2}
Low-density IGZO	5.3×10^{0}

Deep defect levels exist at low density in CAAC-IGZO.

*Reference) M.Tsubuku *et al.*, *SID Symposium Digest*, 44, 166 (2013).

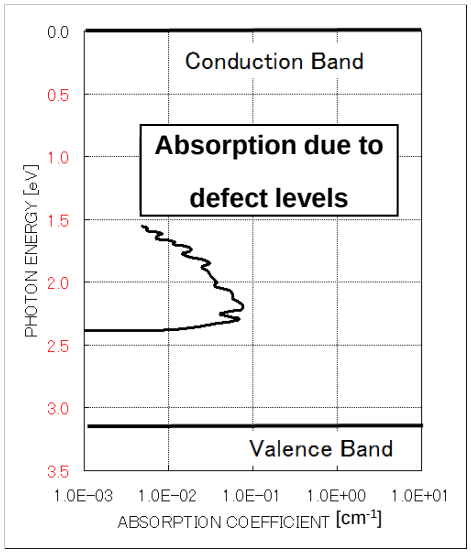
Comparison of Deep Level DOS (density of states) by CPM

amorphous-like IGZO



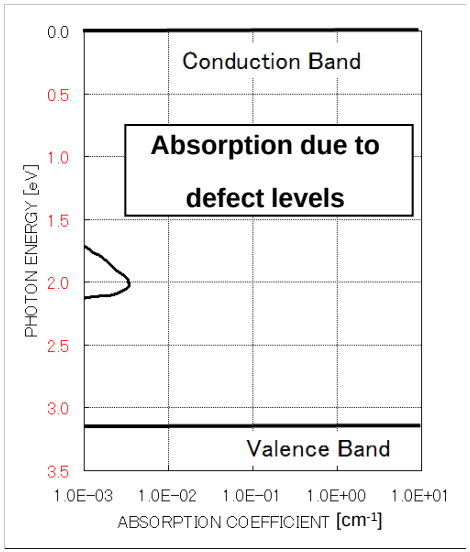
(a) Absorption due to defect levels
5.28 x 10^{-1} [cm^{-1}]

Nano-crystalline IGZO



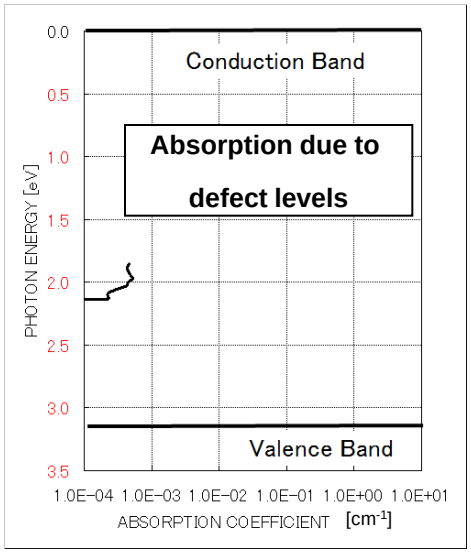
(b) Absorption due to defect levels
1.37 x 10^{-2} [cm^{-1}]

CAAC-IGZO



(c) Absorption due to defect levels
5.86 x 10^{-4} [cm^{-1}]

improved CAAC-IGZO



(d) Absorption due to defect levels
6.17x 10^{-5} [cm^{-1}]

DOS can be reduced to 1/10000 of those of the amorphous-like IGZO which is necessary for LSI.

Therefore, what is found is:
(1)CAAC-IGZO does not have a clear grain boundary.
(2)Grains do exist but they are connected with each.
(3)CAAC-IGZO is an oxide semiconductor film for the lowest DOS (density of states) compared with nc or amorphous-like IGZO.

That is, we think, this CAAC-IGZO has new crystal morphology.
Since CAAC-IGZO does not have a clear grain boundary, any kind of photo-mask patterns can be formed over a large glass substrate in homogeneous or 10-100 nano-meter scale VLSI pattern.

Now, we will examine
“The electrical characteristics of CAAC-IGZO FET”.

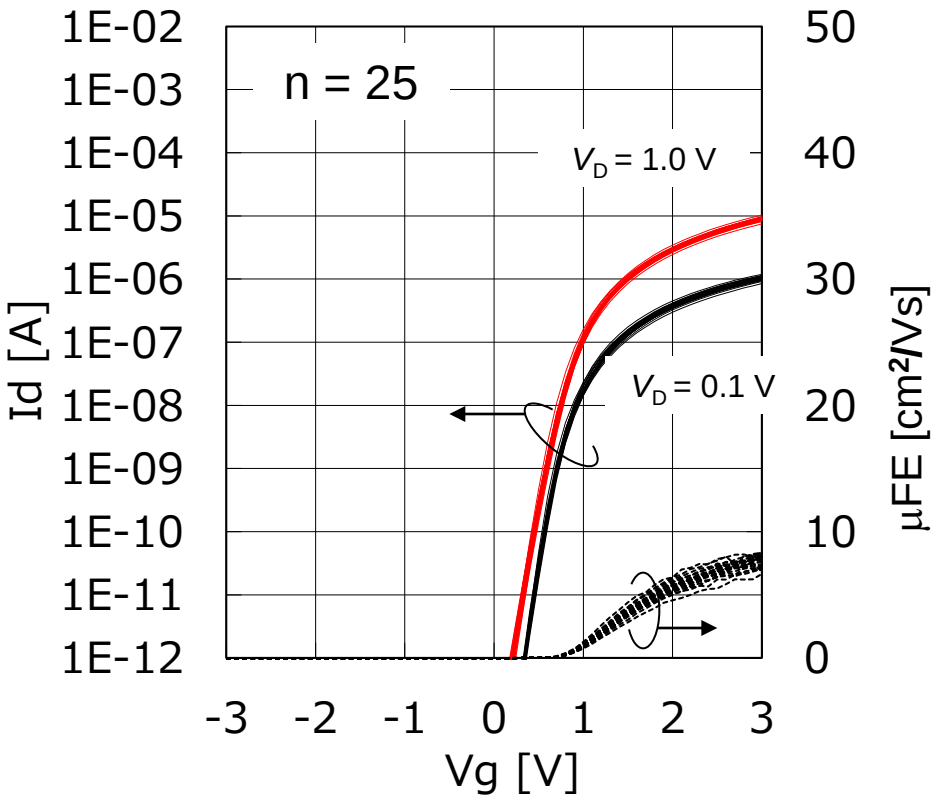
[4] Electrical Characteristics of CAAC-IGZO FET

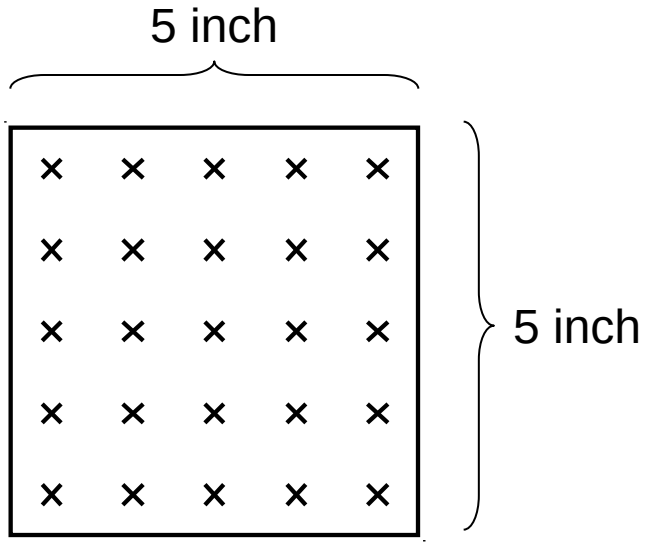
1. Variation in Characteristics of CAAC-IGZO Transistors
2. Dependence of Characteristics of CAAC-IGZO Transistors on Channel Length
3. Temperature Characteristics of CAAC-IGZO Transistors
4. Off-state Current
5. Drain Withstand Voltage of CAAC-IGZO Transistors
6. Reliability Measurement Results
7. Summary of Features of CAAC-IGZO

1. Variation in Characteristics of CAAC-IGZO Transistors

The graph below shows characteristics of 25 CAAC-IGZO transistors in a 5-inch substrate.

L = 0.19 μm, W = 1.0 μm, T_{OX} = 20 nm

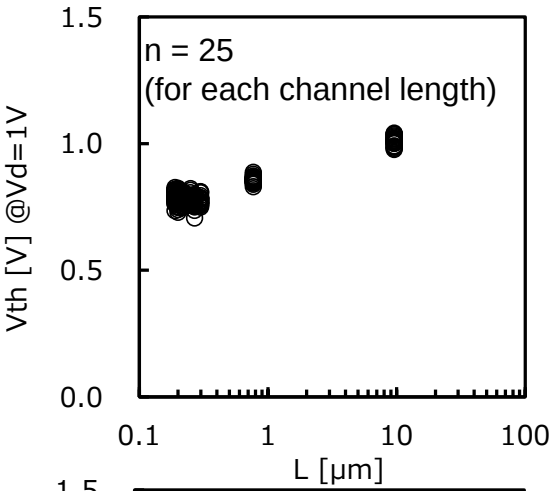


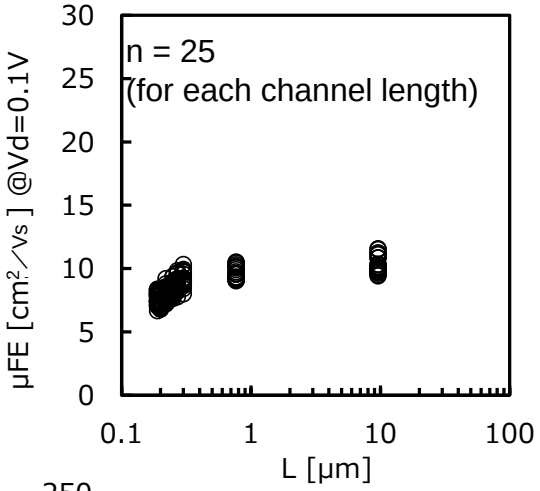


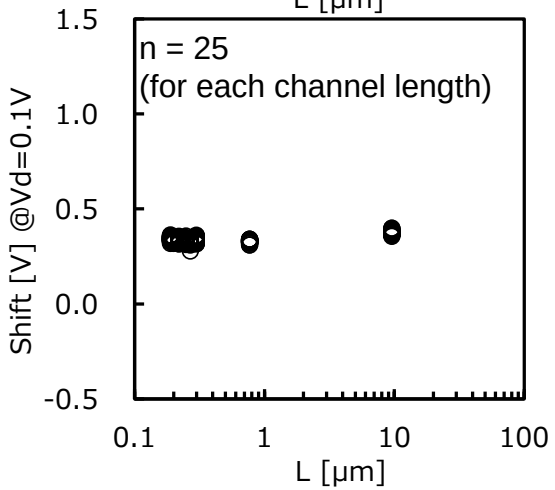
V th (Ave) : 0.79 V
V th (3σ) : 63 mV
S-value (Ave) : 109 mV/dec.
μ (Ave) : 7.7 cm²/Vs

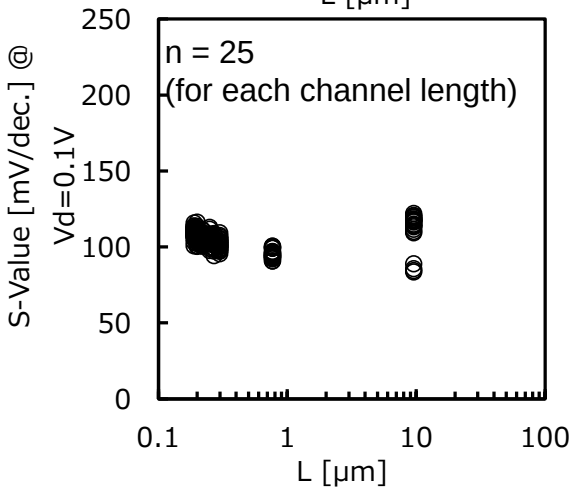
The CAAC-IGZO transistors have excellent uniformity and small S values.

2. Dependence of Characteristics of CAAC-IGZO Transistors on Channel Length









Parameters

Vth : threshold voltage
($\sqrt{I_D}$ extrapolation method, V_D = 1.0 V)

Shift : rising voltage
(gate voltage when $I_D = 10^{-12}$ A, V_D = 0.1 V)

μ_{FE} : field-effect mobility
(V_D = 0.1 V)

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G}\frac{L}{WC_{ox}}\frac{1}{V_D}$$

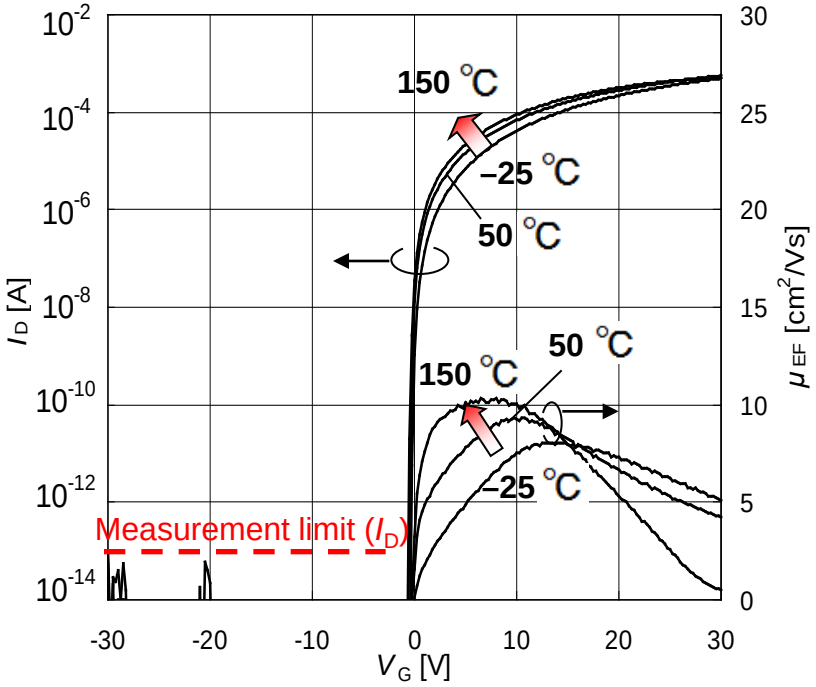
S-Value : S value (V_D = 0.1 V)

$$S = \frac{\partial V_G}{\partial \log_{10} I_D}$$

In the CAAC-IGZO transistors (L = 0.19 to 10 μm, W = 1 μm), each parameter hardly shows dependence on channel length.

3. Temperature Characteristics of CAAC-IGZO Transistors

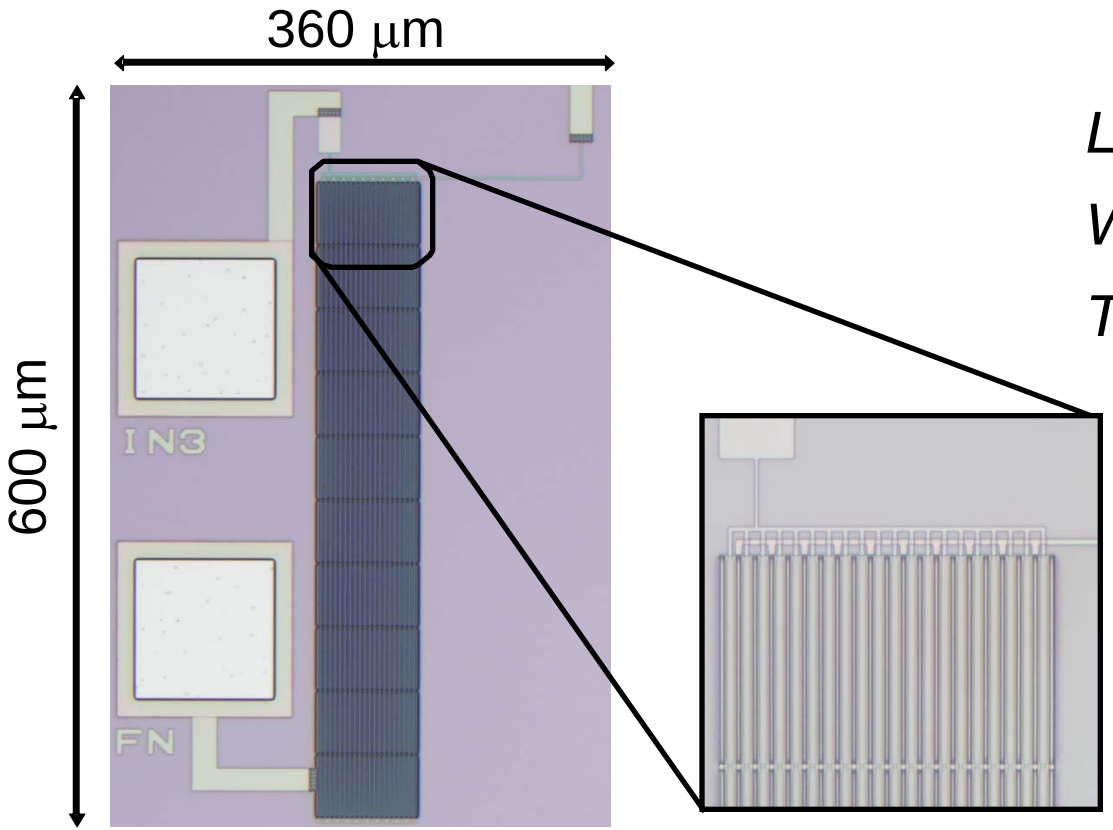
(L = 3.0 μm, W = 20 μm, T_{OX} = 130 nm, V_D = 10 V, T = -25 ℃, 50 ℃, 150 ℃)



Even when temperature is increased, Id-Vg characteristics rises at almost the same positions, which proves the CAAC-IGZO transistor has a favorable characteristics.

The off-state current is smaller than the measurement limit regardless of temperature.

4. Off-state Current



L = 0.44 μm

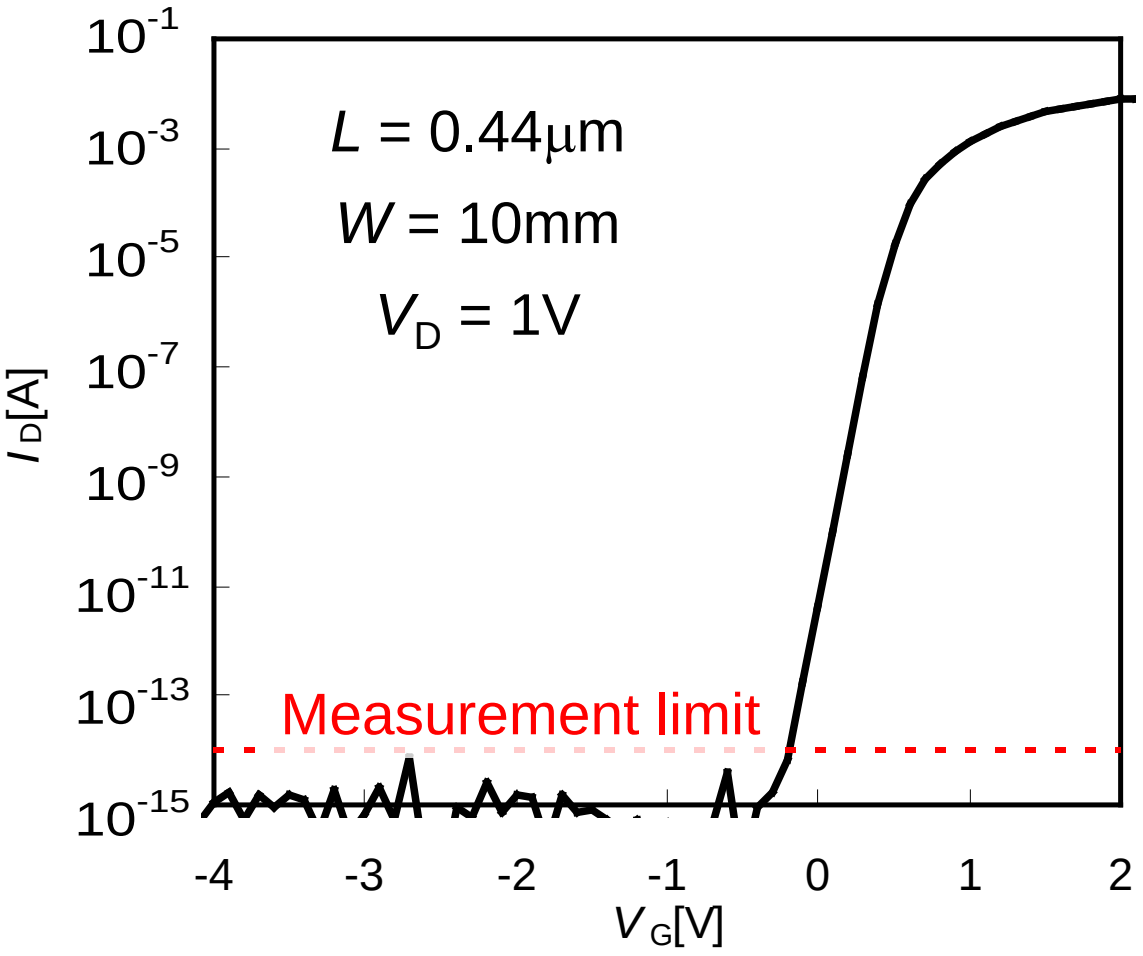
W = 10 mm (10,000 μm)

T_{ox} = 20 nm

200 transistors each with a channel width (W) of 50 μm are connected in parallel.

Micrograph of CAAC-IGZO transistor with a channel width (W) of 10 mm.

Off-State Current of CAAC-IGZO Transistor (L = 0.44 μm)



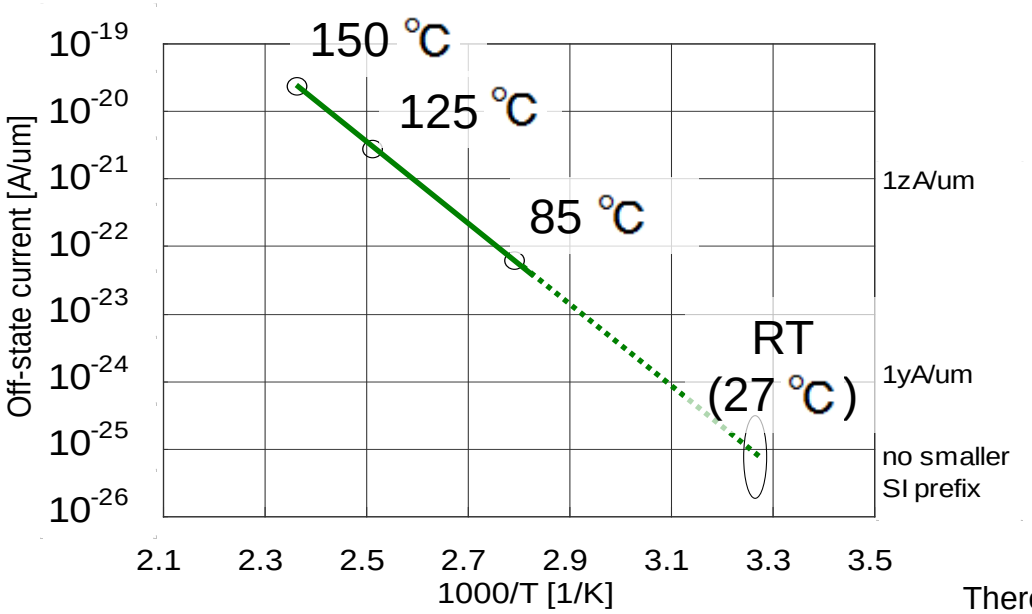
Despite the large channel width (W = 10 mm), the off-state current of the CAAC-IGZO transistor is smaller than the measurement limit.

$I_{off} < 10^{-15}$ A/mm
(10^{-18}A/μm)

A I_D-V_G characteristics of a CAAC-IGZO transistor (L = 0.44 μm, W = 10 mm).

Arrhenius Plot of Off-State Current (L = 0.49 μm)

Because of large Eg of 3.2eV, off-state current is smaller than the level of yA/μm = 10^{-24}A/μm (RT).



m (10^{-3}) A/μm
μ (10^{-6}) A/μm
n (10^{-9}) A/μm
p (10^{-12}) A/μm
f (10^{-15}) A/μm
a (10^{-18}) A/μm
z (10^{-21}) A/μm
y (10^{-24}) A/μm

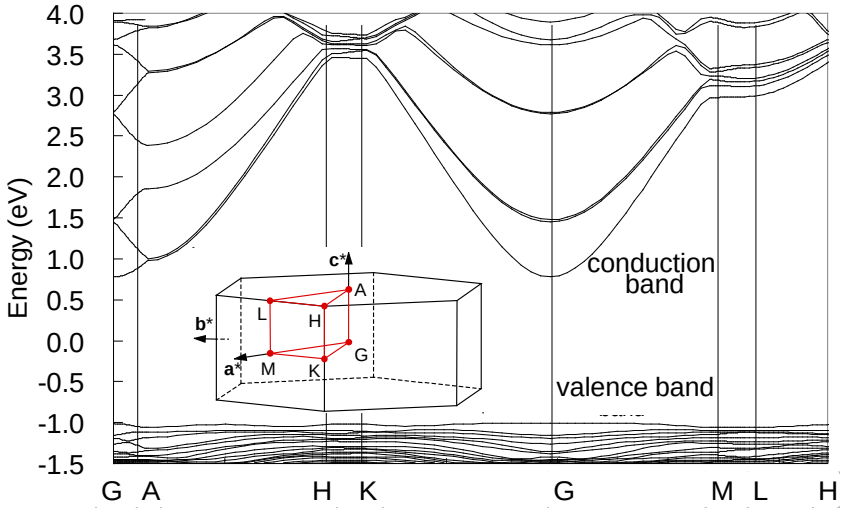
There is no SI (Le Système international d'unités) prefix less than y (yocto)

L = 0.49 μm, W = 10 mm, T_{OX} = 20 nm, I_{off} = Id@Vg = -3V

*Reference) S. Yamazaki, *ECS Trans.*, 54, 85 (2013).

Mechanism of Small Off-State Current

-Brillouin Zone and Effective Mass of Holes in IGZO FET in Off-State -



Brillouin zone (Computer Simulation)

We found a significantly large effective mass of holes of 11 to 41 in IGZO FET, which is 100 times as large as that of 0.25 in Silicon FET.

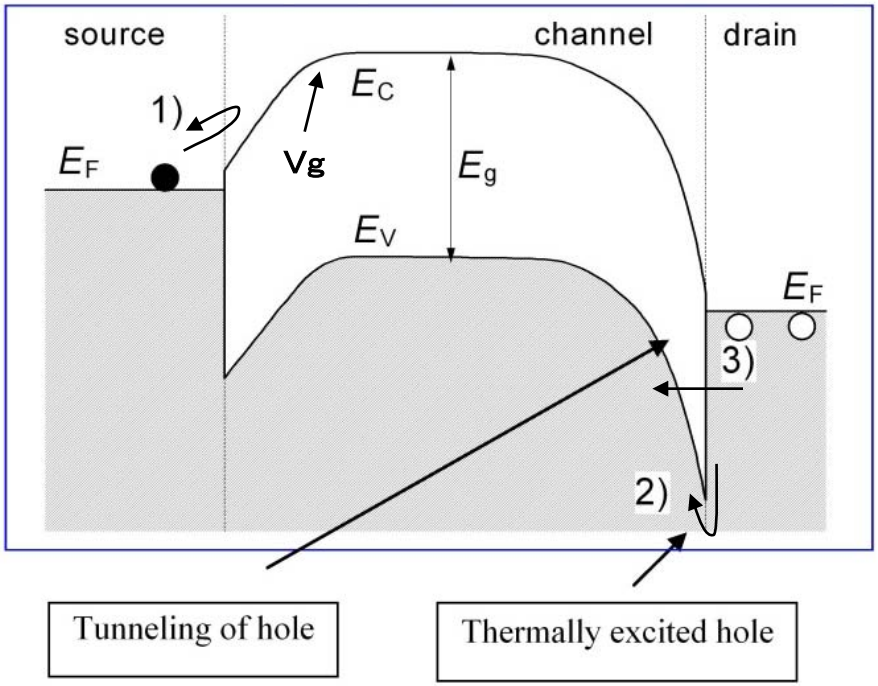
That is, holes are unlikely to move around within IGZO.

Effective mass calculated by the computer simulation

Effective mass of electron m_e^*/m_e	0.25(a*),0.25(b*),0.23(c*)
Effective mass of hole m_h^*/m_e	21(a*),41(b*),11(c*)

*Reference) M. Murakami, *et al*., *Ext. Abstr. Solid States Devices and Materials,* 320 (2012).

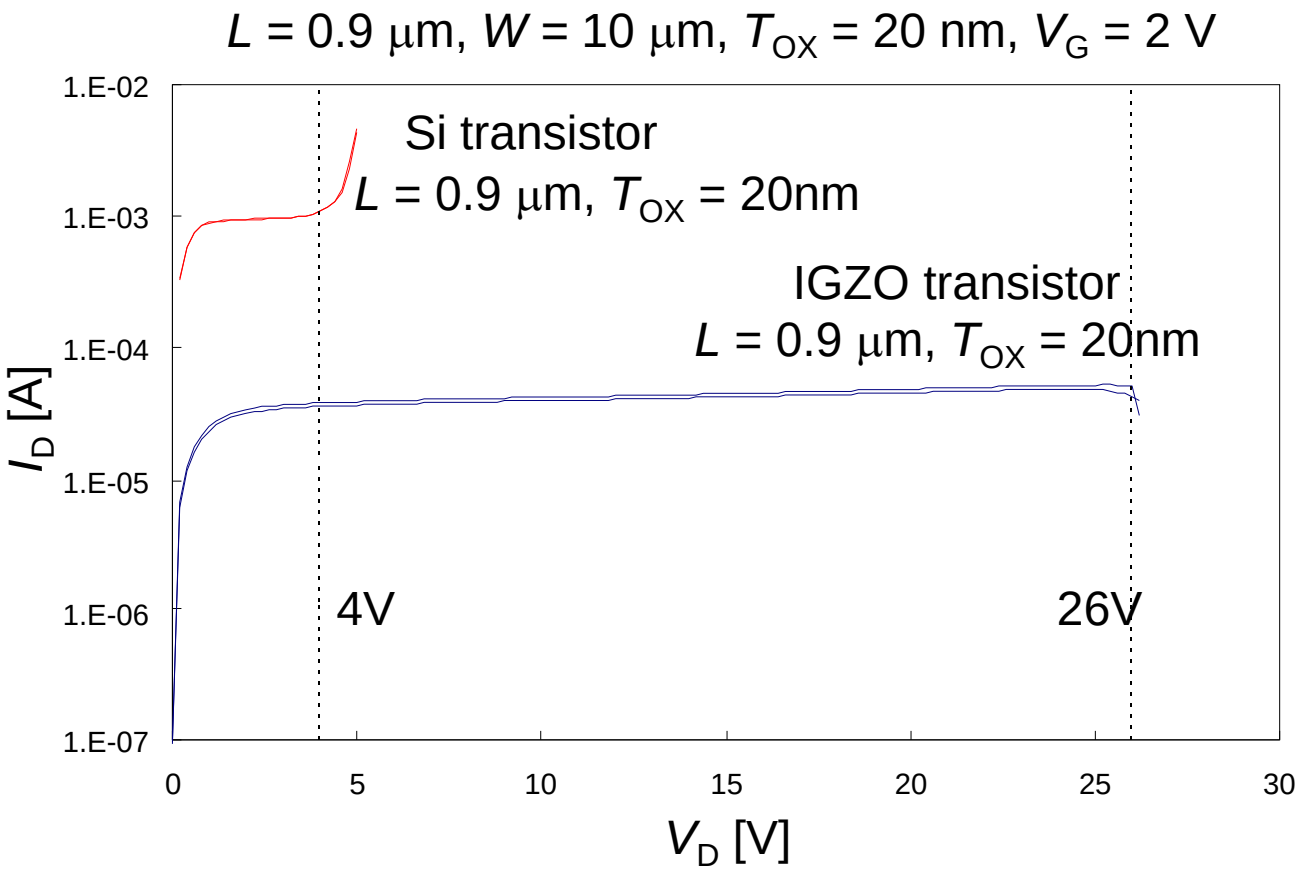
Band Diagram of IGZO FET in Off-State



Band diagram of IGZO FET in off-state :

1) Since Vg is reverse biased, no electrons flows from source.
2) In the reverse bias state, holes which are minority carriers from drain has a large effective mass; therefore, the current due to holes hardly flows. Tunneling current and thermally excited holes are both negligible.
3) As a result, the off-state current is extremely small.

5. Drain Withstand Voltage of CAAC-IGZO Transistors



Unlike in the Si transistors, avalanche breakdown does not occur in the CAAC-IGZO transistors.

6. Reliability Measurement Results

B (Bias)-T (Temperature Treatment) and Hot carrier injection

	Central portion of Substrate	End portion of Substrate	⊿Ids
+GBT Vg=+3.3V 125℃	⊿Vth=0.11V @12hr ⊿Ids=10.5% @12hr	⊿Vth=0.13V @12hr ⊿Ids=10.7% @12hr	0.001 year
−GBT Vg=−3.3V 125℃	⊿Vth=0.00V @12hr ⊿Ids=0.0% @12hr	⊿Vth=−0.03V @12hr ⊿Ids=−1.7% @12hr	0.001 year
HCI Vd=+3.3V 25℃	⊿Vth=0.02V @12hr ⊿Ids=0.8% @12hr	⊿Vth=0.01V @12hr ⊿Ids=0.8% @12hr	0.001 year

L = 0.8μm, W = 10μm, T_{ox} = 20nm

■ Central portion of Substrate ◇ End portion of Substrate

Reliability Measurement Results

⊿Ids (*)Deterioration rate of Ids with 3.0V of Vd and 3.0V of Vg

+GBT Vg=+3.3V 125℃	⊿Ids at 0.001 year (*) Target specification: ≦10% at 0.001 year	Central portion: 10.0 % at 0.001 year	measurement result	Central portion: ○
		End portion: 9.9 % at 0.001 year		End portion: ○
-GBT Vg=-3.3V 125℃	⊿Ids at 0.001 year (*) Target specification: ≦10% at 0.001 year	Central portion: 0.0 % at 0.001 year	measurement result	Central portion: ○
		End portion: -1.5 % at 0.001 year		End portion: ○
HCI Vd=+3.3V 25℃	⊿Ids at 0.001 year (*) Target specification: ≦10% at 0.001 year	Central portion: 0.9 % at 0.001 year	measurement result	Central portion: ○
		End portion: 0.9 % at 0.001 year		End portion: ○

7. Summary of Features of CAAC-IGZO

	CAAC-IGZO (intrinsic)	Si (intrinsic)	Difference
• Eg→wide	2.8 to 3.2 eV	1.1 eV	
• Minority carrier (hole)	$< 10^{-9}$ cm^{-3}	10^{11} cm^{-3}	10^{20}
• Majority carrier (electron)	Injection from only source		
• Avalanche breakdown	non	occurs	
• Debye Length	> 1 m	μm order	$> 10^{8}$
• Reliability	high (same level of Si LSI)		
• Off-state current	yA/μm order (at 85 °C)	pA/μm order	
• Small S value, close to an ideal value	60 to 120 mV/dec.		
• On/off ratio	$> 10^{17} \sim 10^{20}$	10^{6} to 10^{10}	

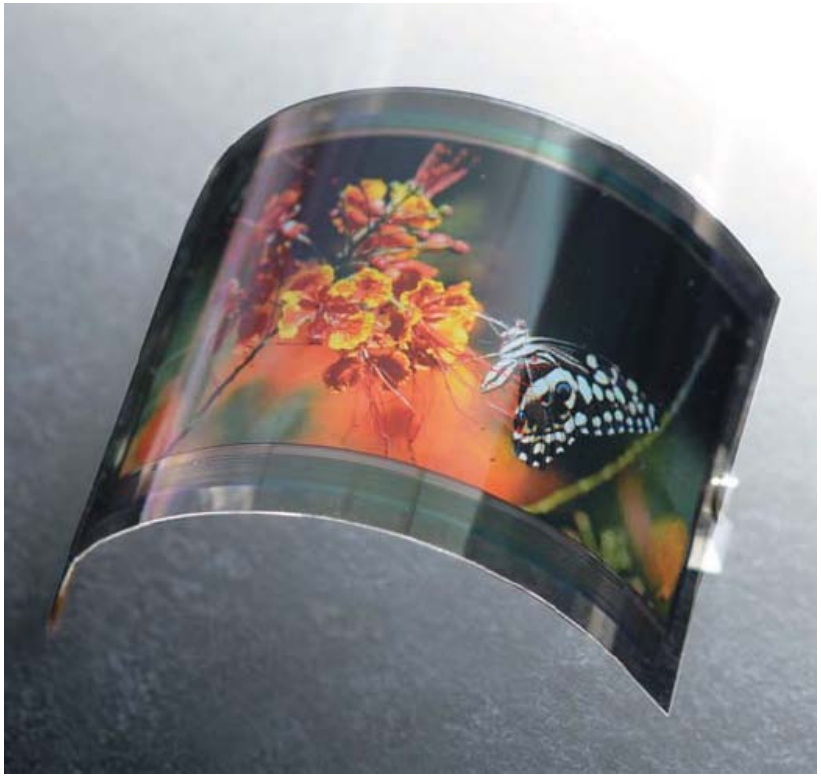
[5] Applications of Display and VLSI

13.5-Inch 4K OS-FET OLED Display

Specifications

Screen Diagonal	13.5-inch
Driving Method	Active Matrix
Resolution	3840 x RGB x 2160 (QFHD)
Pixel Density	326 dpi
Aperture Ratio	55.8%
Pixel Arrangement	RGB Stripe
Source Driver	Chip on Film
Gate Driver	Integrated
Number of OS-FETs	1.25×10^8

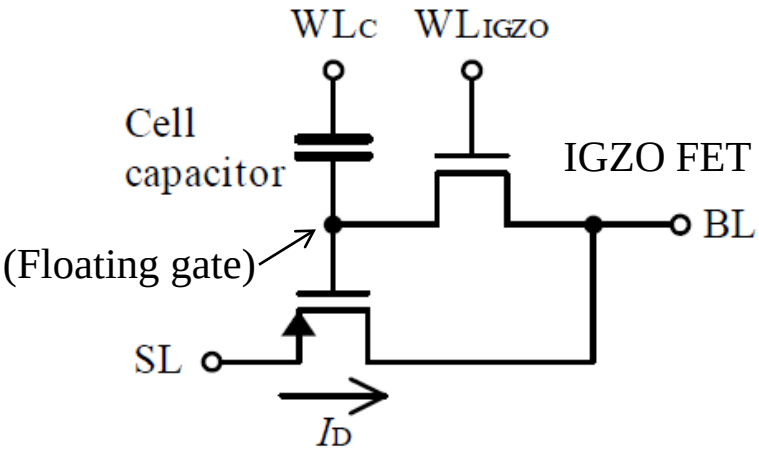
3.4-Inch High-Definition Flexible OLED Display



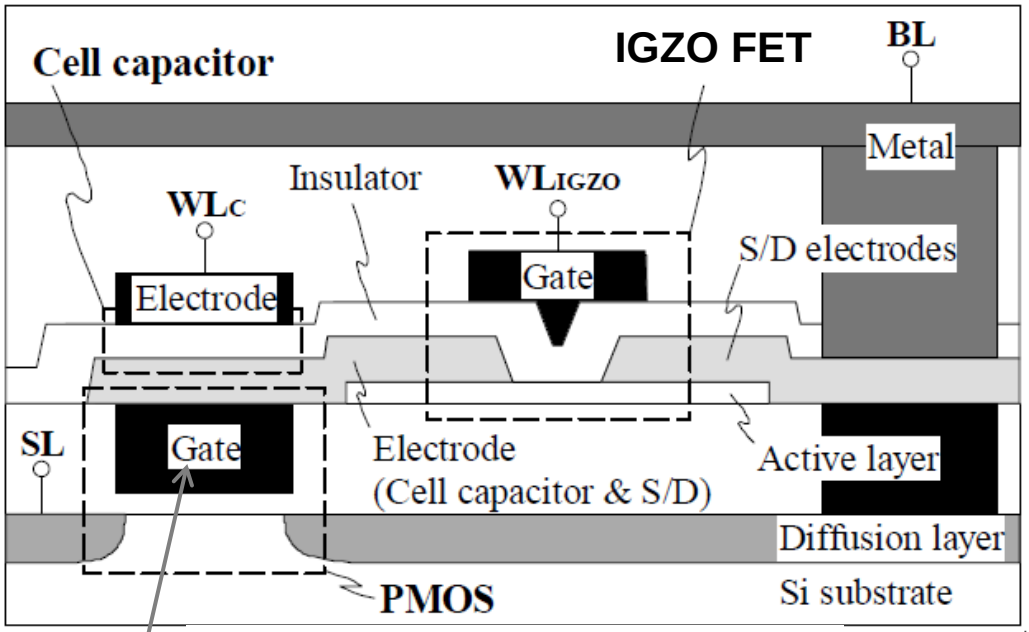
Specifications

Screen Diagonal	3.4-inch
Driving Method	Active Matrix
Resolution	960 x RGB x 540 (qHD)
Pixel Density	326 dpi
Aperture Ratio	40%
Pixel Arrangement	RGB Stripe
Coloring Method	White OLED with Color Filters
Source Driver	Integrated
Gate Driver	Integrated
Number of OS-FETs	1.67×10^6

NOSRAM cell structure



(a) Circuit diagram.

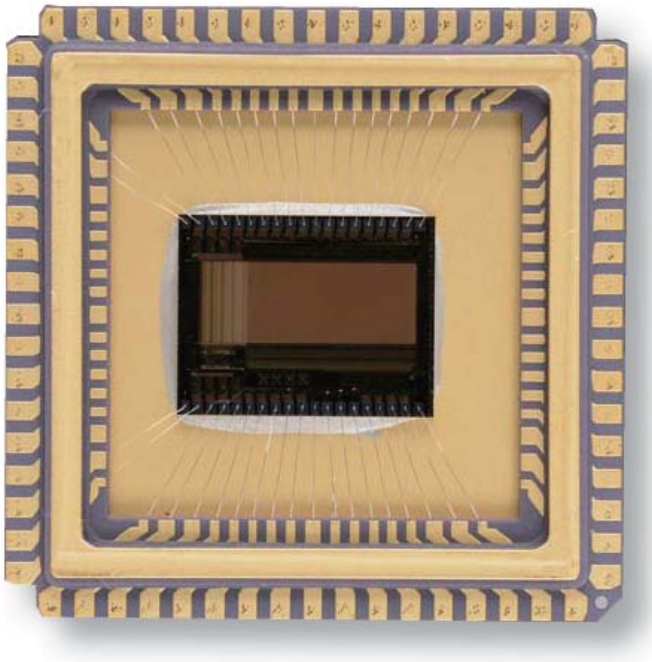


(b) Cross-sectional view.

*Reference) H. Inoue *et al., IEEE J. Solid-St. Circ.*,**47** (2012).

NOSRAM

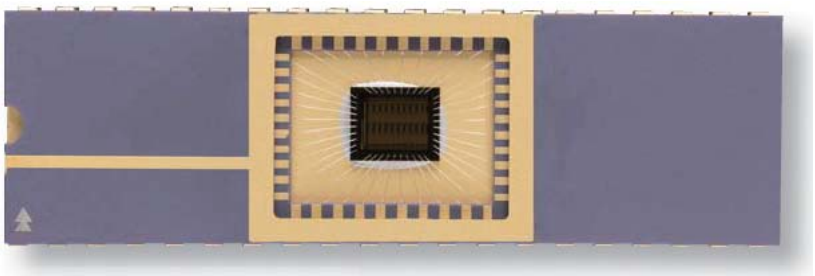
Specifications



Memory Capacitance	1 Mbit
Technology (Channel length)	Si-FET : 0.8 μm
	CAAC-IGZO FET : 0.8 μm
Die size	4.9 mm x 6.4 mm
Cell size	4.4 μm x 2.8 μm
Organization	1024 bit/page x 1024 pages
Power supply voltage	VDD / VH / VL = 3 V / 4.5 V / -1 V
Write Time	150 ns/page
Read Time	900 ns/page
Retention Time	> 60 days (at 85 ℃)
Number of FETs (Si)	1,190,000
Number of FETs (OS)	1,050,000

*Reference)
H. Inoue *et al., JSSC*, 47 (2012) 2258.
S. Yamazaki *et al., Proc. SID'12 Dig.* (2012) pp. 183-186.
S. Nagatsuka *et al., in 5th IEEE Int. Memory Workshop* (2013).

FPGA (Field Programmable Gate Array)

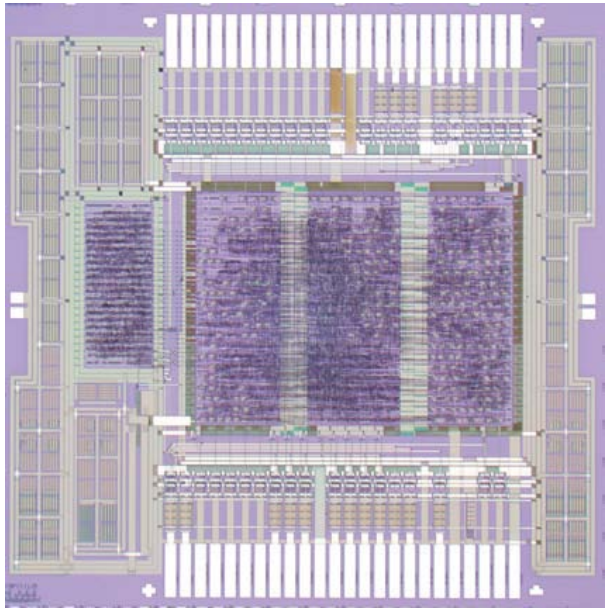


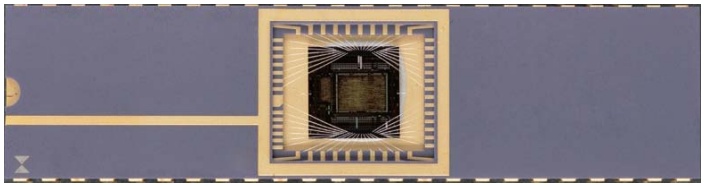
Specifications of MC-DRPLD.

Core Size of MC-DRPLD	2.6 x 4.4 mm
Number of the PLEs	20
Number of the User I/O pins	20
Configuration Memories	7,520 bits
Look-Up Table inputs	4
Power Supply Voltage	2.5-3.3 V
Channel Length: CMOS FET / CAAC-IGZO	0.5 μm / 1.0 μm
Number of FETs (OS)	9,040
Number of FETs (Si)	45,411

*Reference)
Y. Okamoto *et al*., UCSIC and TFT poster session (2013).

8-Bit Normally Off CPU



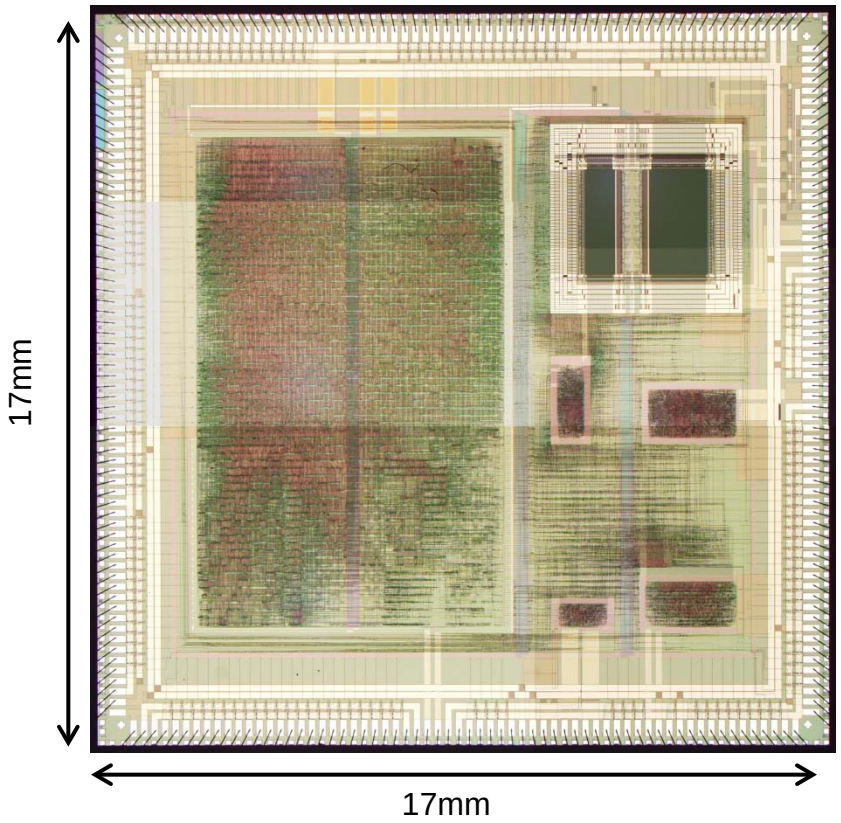


Specifications

Architecture	8bit CISC
Technology (Channel length)	Si-FET : 0.5 μm
	CAAC-IGZO-FET : 0.8 μm
Die size	8.4 mm x 12.0 mm
Core size	4.5 mm x 3.4 mm
Clock frequency	25 MHz
Power supply voltage	2 V
Number of FETs (OS)	255
Number of FETs (Si)	42,500

*Reference)
T. Ohmaru *et al*., *Ext. Abstr. Solid States Device and Materials* (2012) pp. 1144-1145.
H. Kobayashi *et al*., *COOL Chips XVI* (2013).

32-Bit Normally Off CPU



*Reference) N. Sjokvist *et al.*,"Zero Area Overhead State Retention Flip Flop Utilizing Crystalline In-Ga-Zn Oxide Thin Film Transistor with Simple Power Control Implemented in a 32-bit CPU“, to be published in SSDM 2013 Session M-6-4.

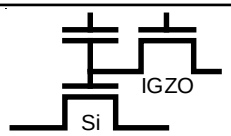
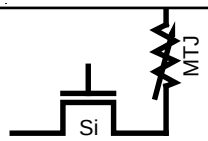
Specifications

Technology	Si	0.35 μm (GI: 10nm)
	IGZO	0.8 μm (GI: 20nm)
Number of FETs (OS)	51,410	
Number of FETs (Si)	372,000	
Clock frequency	15MHz	
Power supply voltage	Si	2.5 V
	IGZO	3.5 V
ISA	32-bit RISC	
Pipeline	3 stages	
IOPAD	256	

Cache

Organization	Unified I and D cache
Block size	1 word (= 4 bytes)
Hit time	1 clock cycle
Size	2KB
Block placement	2-way
Replacement policy	LRU
Write strategy	Write back

[6]Comparison of OS FET to MRAM & NAND Flash Memory

	OS Memory	STT-MRAM	NAND Flash memory
Non-volatility	Utilizes small off-state current	Utilizes spins	Charge retention of floating gate
Materials	OS material	Magnetic rare earthes	Si
Driving method	Voltage-driving (4-pin)	Current-driving (2-pin)	Voltage-driving (4-pin)
Power consumption	On/off control of FET	Spin-directions charge of magnetic body	Charge injection to floating gate
Writing energy	4fJ/bit (Charging/discharging of capacitance)	90fJ/bit (Joule heat)	1.4nJ/bit (Injecting charge)
Writing degradation	No	Yes	Yes
Cell size	$11F^2$~	$8F^2$ ~	$4F^2$ ~
Multivalued	Possible	Difficult	Possible
3D conversion	Possible	Difficult	Possible
Magnetic-field resistance	high	low, magnetic-field interference*	high
Circuit diagram			

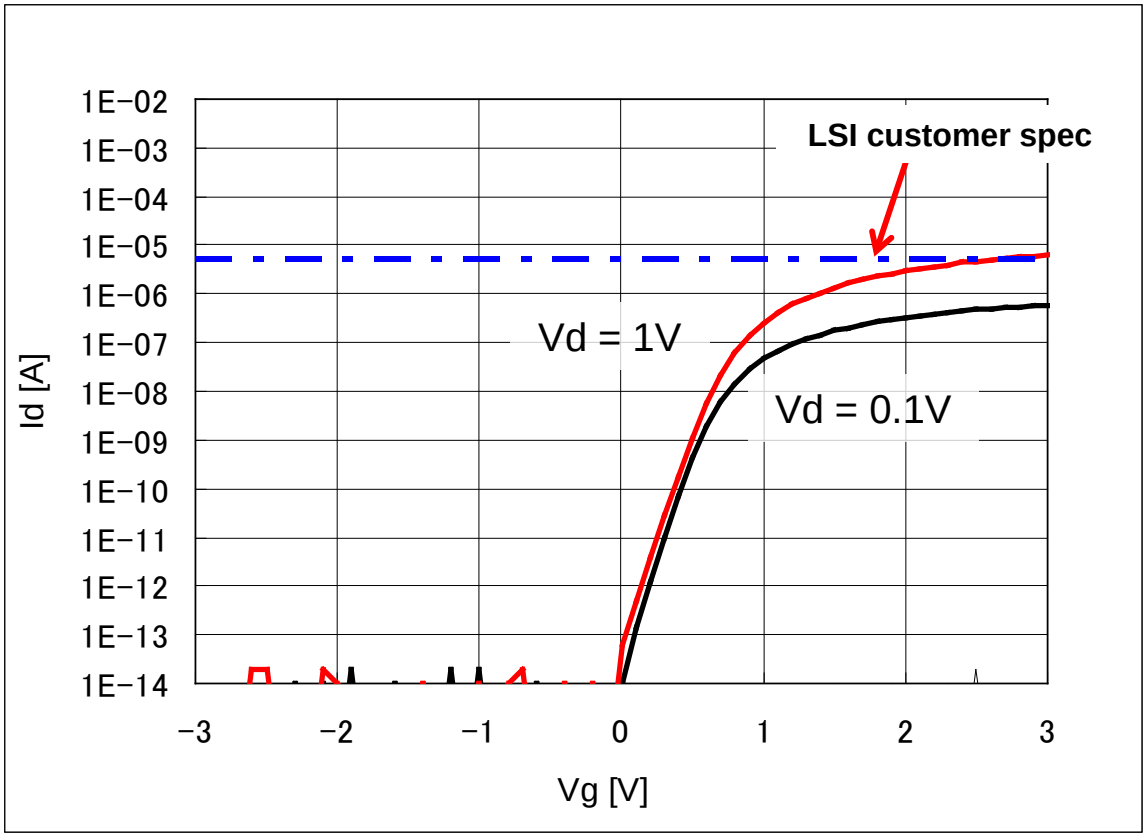
*magnetic-field interference ; voltage driving 4 terminal electric network

[7] Conclusion

1. We believe CAAC-IGZO has “new crystal morphology”.
2. This is because IGZO does not have a clear grain boundary.
3. Reliability of CAAC-IGZO is acceptable for VLSI spec.
4. IGZO semiconductor has an extremely low off-state current. Then, by integrating CMOS of the Si semiconductor, we attained an ideal switch (off-state current is completely stopped).
5. Application forms of CAAC-IGZO are, for example, CPU, Non-volatile memory (NOSRAM) without fatigue, and FPGA.
6. We believe CAAC-IGZO technology can achieve new innovation in VLSI industry.

Recent Topics

Id-Vg Characteristics of CAAC-OS FET (L/W = 40nm/40nm)



Designed: L/W = 40nm/40nm
Finish : L/W = 68nm/34nm

Condition for measurement	Measured Value
Ion [μA] @Vd=1V,Vg=2.7V	6.46 μA
Vth [V] @Vd=1V	0.57 V
S-value [mV/dec] @Vd=0.1V	104.4 mV/dec

Thank you for your attention.

- We express great appreciation to
  Dr. Noboru Kimizuka, the first to synthesize IGZO in the world.

- His research outcome now grows to industry by CAAC-IGZO discovery.

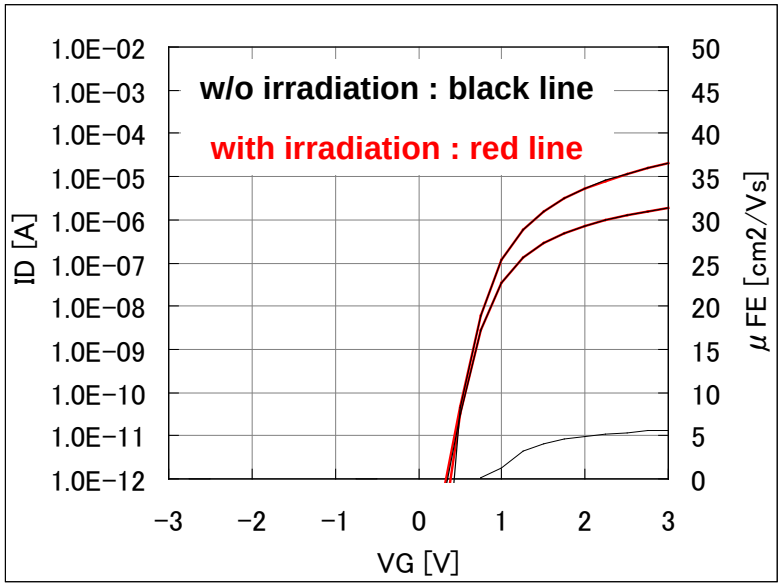
- We believe 40nm channel length FET using CAAC-IGZO shall open the door to the high definition 3D VLSI.

SEL
SEMICONDUCTOR ENERGY LABORATORY

Influence of Light Irradiation

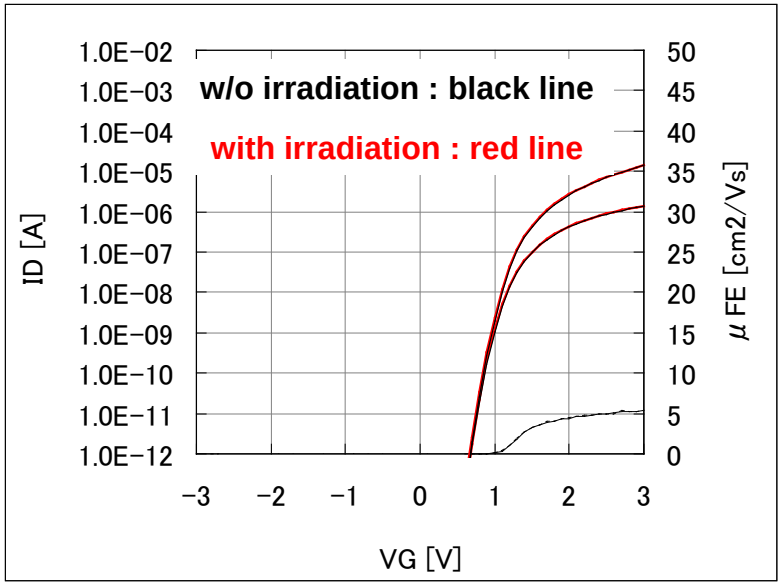
Id-Vg characteristics under light irradiation

Monochromic UV light



The photon flux：7 x 10^{15} $cm^{-2}s^{-1}$
Wavelength of Light : 350 nm

White LED



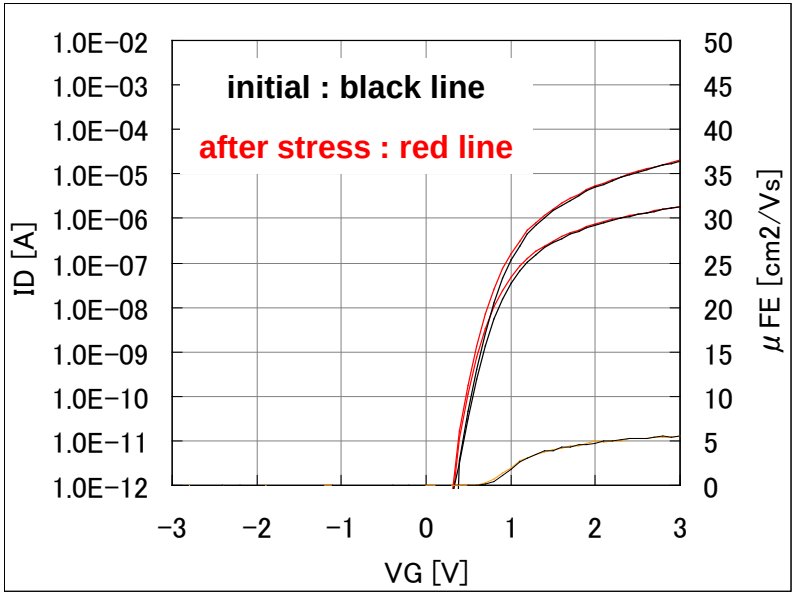
Illumination Intensity : 40000lx

L = 1μm, W = 10μm, T_{ox} = 20nm

Negative-Bias Photodegradation

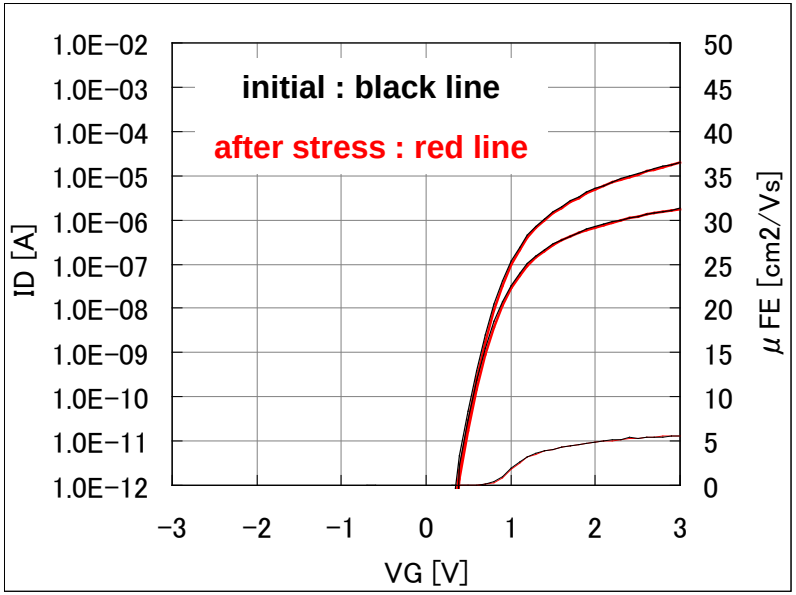
Degradation under negative bias temperature illumination stress (NBTIS)

Monochromic UV light



Gate Bias Stress : -3.3V
Stress temperature : 40 °C
Stress Time : 1hr
The photon flux : 7 x 10^{15} $cm^{-2}s^{-1}$
Wavelength of Light : 350 nm

White LED



Gate Bias Stress : -3.3V
Stress temperature : 40 °C
Stress Time : 1hr
Illumination Intensity : 40000lx

L = 1μm, W = 10μm, T_{ox} = 20nm