Circuit and System Design Semiconductor and Nano Technology Test and Verification PCB and PWB Technology Micro-Electro-Mechanical System MEMS Electronic Design Automation Technology Bioelectronics Innovations IC Packaging Technology Photovoltaic Technology and Manufacturing Circuit and System Design Semiconductor and Nano Technology PCB and

asQED Symposium 2010

2nd Asia Symposium on Quality Electronic Design

3 & 4 Aug 2010
Gurney Hotel
Penang, Malaysia

Co-organized By

MiGHT
Malaysian Industry-Government Group for High Technology

isQED www.isqed.org

MIMs
Malaysia Institute of Microsystems (MIMs)

Supported By

MIDA

MOSTI

ASQED 2010 Keynotes & Speakers Review

State of Global Semiconductor Industry

Richard Goldman, Vice President Corporate Marketing & Strategic Alliances, Synopsys Inc. Rich is responsible for overseeing all interoperability programs and partnering programs with semiconductor vendors, IP providers, and platform vendors as well as the Synopsys worldwide university program. He also serves as CEO of Synopsys Armenia and is responsible for all aspects of the operation of Synopsys Armenia. Rich is a guest Professor at the Chinese Academy of Science, and is a Commissioner of the Advanced SOC Design Joint Lab Academic Committee there. Currently, He chairs the EDAC Interoperability and Quality Committee. Rich served as co-chair of the RAPID Board of Directors and was a member of the EIA/EDIF Steering Committee.

Bio-inspired Electronics based on Spin and Dipole Fluctuated System

Dr. Hitoshi Tabata, Professor, Head of Department of Bioengineering, The University of Tokyo. The keynote highlights the creation of a new-type electronics known as iotronics) is learned from bio fluctuations. An example is a controllable physical fluctuation system. He received a Japan Society for the Promotion of Science(JSPS) Prize in 2008. His current research is in the area of "Nano-Bioelectronics", "Artificial superlattices of functional oxides" and "Spin electronics and multi ferrotronics" He is a member of Material Research Society, and Japan Society of Applied Physics.

Analog IC Market Trends: The OLD becomes NEW again

Paul Emerson, General Manager New Business Providing Grounds, HVAL, Texas Instruments. Market trends, which consider both "old" and "new" industries, will be presented to highlight areas that governments, corporations, and individuals will focus their time and investments in the years to come. Analog IC design methodologies, process technologies, and development trends will be presented to show how industrial leaders will realize their next generation innovative analog IC products. He is also an analog designer and the inventor or co-inventor of 7 patents in Hard-Disk drive Preamp circuit design.

Cost-effective Road to Zero Defects

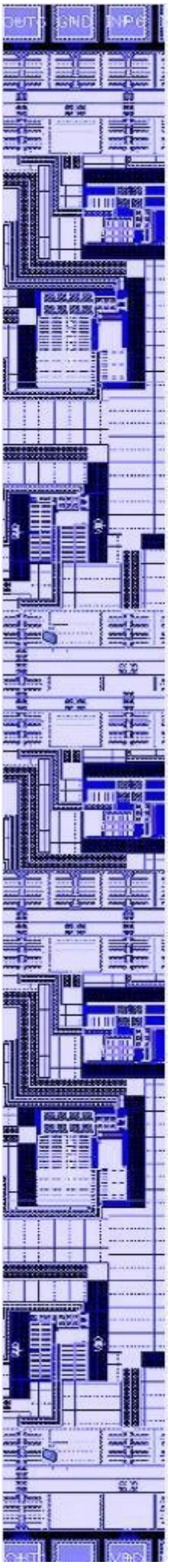
Sanjiv Taneja, Vice President, Encounter Test business, Cadence Design Systems. Under his leadership for the last two-and-a-half years, Cadence's Test business has emerged in a stronger strategic, technological and product positions through a holistic strategy for manufacturing Test and deep, collaborative relationships with its customers and Test ecosystem partners. Mr. Taneja started his career at Bell Labs in Murray Hill, NJ where he spent over 13 years in EDA software development and led the Custom/Analog Layout Automation group prior to the acquisition of Bell Labs Design Automation group by Cadence in 1998. Mr. Taneja holds a BS degree in Electrical Engineering from Indian Institute of Technology, New Delhi, a MS degree in Computer Science from Ohio State University, and MBA from New York University.

Leveraging parallel processing in SoCs

Dr. Jeroen Leitgen, Co-Founder and Chief Technology Officer, Silicon Hive. Jeroen has 15 years experience in parallel computer architectures and reconfigurable computing. At Silicon Hive he has been leading the development of Silicon Hive's parallel processing technology and related processor generation tools and libraries. At present he is responsible for all world-wide research and development within Silicon Hive.

Luncheon's Speech - Neuromorphics: The reality of nanoscale devices as part of future System On System (SoS) Integration

Prof. Kamran Eshraghian, founder and President of Eshraghian Laboratories Pty Ltd (ELabs). ELabs is a virtual platform for cutting-edge research into nano-based and micro-based technologies. He is best known in the international arena as the "grandfather" of CMOS VLSI Design. He has held faculty positions in Elelctronic Engineering and Computer Science in Australia, United States and Europe. A distinguished world expert in the field of VLSI systems and circuits, has held over 40 patents and co-authored 5 textbooks. His achievement is encapsulated in standard text "Principles of CMOS VLSI Design: A Systems Perspective", used in over 800 universities through the world.



ASQED 2010 Tutorial and Speakers Review

Dr. Tanay Karnik - **Terascale Computing and Interconnect Challenges: 3D Stacking Considerations.** Dr. Tanay Karnik (M'88, SM'04) received his Ph.D. in Computer Engineering from the University of Illinois at Urbana-Champaign in 1995. His research interests are in the areas of variation tolerance, power delivery, soft errors and physical design. He has published over 40 technical papers, has 39 issued and 36 pending patents in these areas. He received an Intel Achievement Award for the pioneering work on integrated power delivery. He has presented several invited talks and tutorials, and has served on 5 PhD students' committees. He was a member of DTTC, DAC, ICCAD, ICICDT and ISQED program committees and JSSC, TCAD, TVLSI, TCAS review committees. Tanay is the General Chair of ISQED'08 and ICICDT'08. He is also appointed the Technical Program Chair for ASQED 2009 (Malaysia).

Prof. Albert Wang - **ESD + RFIC Co-Design for Whole-Chip Design Optimization** IEEE Fellow, Dept of Electrical Engineering, University of California. Prof. Wang's research interests center on RF/Analog/Mixed-Signal Integrated Circuits, Design for Reliability for ICs, SoC, IC CAD and Modeling, Emerging technologies, etc. His academic credits include one book entitled "On-Chip ESD Protection for Integrated Circuits" (Kluwer, 2002), 150+ peer-reviewed papers and several U.S. patents. He received the BSEE degree from Tsinghua University, China, and PhD EE degree from State University of New York at Buffalo, in 1985 and 1996, respectively. From 1995 to 1998, he was with National Semiconductor Corp. in the Silicon Valley. From 1998-2007, he was a professor at the Illinois Institute of Technology, (Electrical & Computing Engineering). Since 2007, he is a professor at the University of California and Director for the Laboratory for Integrated Circuits and Systems.

Dr. Rajiv V. Joshi - **Planar and Nonplanar Structures Thermal Modelling Studies,** Dr. Rajiv is currently a Research Scientist, IBM T.J. Watson Research Center NY. Dr. Rajiv V. Joshi is involved in the development of metallization schemes for VLSI circuits. He obtained his PhD (1990) at the Columbia University, New York, Masters of Engineering (1981) Manufacturing Science and the Massachusettes Institute of Technology Cambridge, Masters of Science (1979) Mechanical Engineering, University of Maine, Maine, Orono and Bachelor Science (1977), Mechanical Engineering, Indian Institute of Technology, Bombay, India. He had specific training in custom integrated design of VLSI in IBM, and works extensively in VLSI design, microelectronics, materials science at MIT and Columbia University. His recent awards include IEEE/ACM William J. McCalla ICCAD Best Paper Award ICCAD 2009, & Outstanding Contribution Award for Statistical Methodology and tool (2008).

David W. Bergman - **IPC Standards and Electronics Manufacturing Environment.** Vice President, International Relations, IPC (Association Connecting Electronics Industries) He has worked at IPC for over 30 years of which more than 25 were as part of the staff team responsible for IPC standardization efforts, education and certification programs. In his current role in International Relations, David is responsible for the globalization effort s of IPC including IPC's China staff and representatives in Europe and Russia. David is also responsible for joint activities with related sister organizations and was selected to serve 10 years as Secretary General of the World Electronic Circuit Council. In recognition of his efforts to identify alternatives to CFCs for defluxing Printed Wiring Board Assemblies, David was awarded the U.S. EPA's Stratospheric Ozone Protection Award as well as EPA's "Best of the Best" Stratospheric Ozone Protection Award.

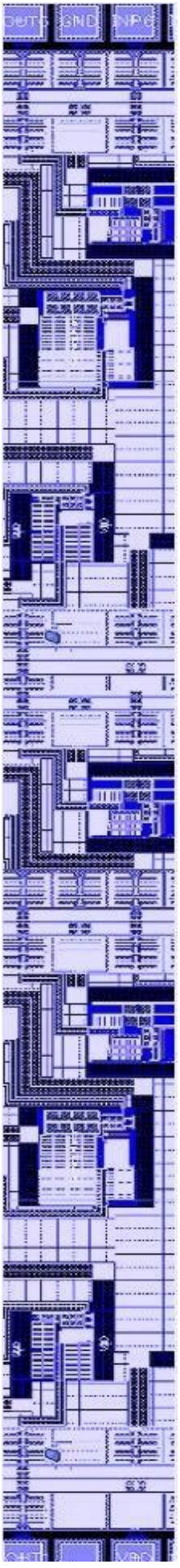
Corporate Sponsors

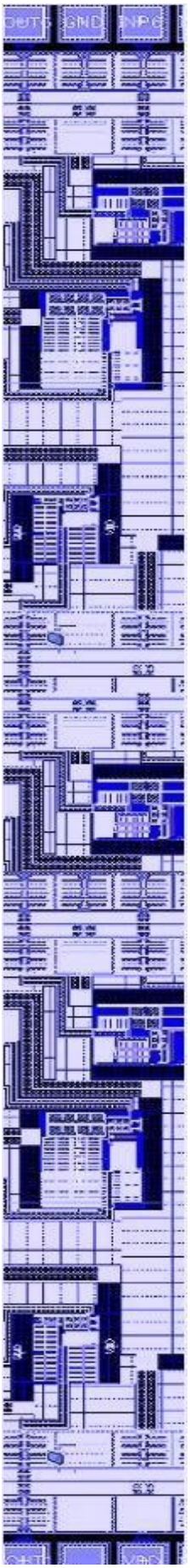
cadence™ SYNOPSYS®

For Sponsorship & Exhibit participation and info contact Ms. Chin, kimlai@shrdc.org.my +603-55133560

CONFERENCE AT A GLANCE 3 - 4 August 2010 Penang

MONDAY	**2 AUG**			
6pm—8pm	Pre-registration			
TUESDAY	**3 AUG**			
7:30am	Registration			
8:30am	Opening Speech by Founder and Chairman			
9:00am	Keynote 1 : Richard Goldman, Synopsys			
10:00am	Tea Break & Networking Session			
10:30am	Opening Ceremony by Minister (Malaysia)			
11:35am	Keynote 2 : Dr. Hitoshi Tabata, The University of Tokyo			
12:30noon	Buffet Lunch			
1:30pm	Break-out & Embedded Tutorial Parallel Sessions			
	Room A	Room B	Room C	Room D
	Session 1A	Session 1B	Session 1C	Tutorial 1D
3:30pm	Tea Break and Networking Session			
	Break-out & Embedded Tutorial Sessions			
	Room A	Room B	Room C	Room D
	Session 2A	Session 2B	Session 2C	Tutorial 2D
5:30pm	End of ASQED 2010 Day 1			
WEDNESDAY	**4 AUG**			
7:30am	Registration			
8:30am	Keynote 3 : Paul Emerson, Texas Instruments			
9:30am	Keynote 4 : Sanjiv Taneja, Candence Design Systems			
10:30am	Tea Break & Networking Session			
11:00am	Keynote 5 : Jeroen Leitgen, Silicon Hive			
12:00noon	Buffet Lunch			
	Luncheon Speech by Prof. Kamran Eshraghian, Eshraghian Laboratories			
1:30pm	Break-out & Embedded Tutorial Parallel Sessions			
	Room A	Room B	Room C	Room C
	Session 3A	Session 3B	Session 3C	Tutorial 3D
3:30pm	Tea Break and Networking Session			
	Room A	Room B	Room C	Room D
	Session 4A	Session 4B	Session 4C	Tutorial 4D
5:30pm	End of ASQED 2010 Day 2			
THURSDAY	**5 AUG**			
Optional 1 Day Tour of Penang Attractions and Industrial Visit				





Sessions (Tentative Schedule)

Session 1A	Circuit and System Design
Session 1B	Circuit and System Design
Session 1C	IC Packaging Technology
Tutorial 1D	Dr. Tanay Karnik , INTEL
Session 2A	PCB and PWB Technology and Manufacturing
Session 2B	Semiconductor and Nano Manufacturing
Session 2C	Bioelectronics Innovations
Tutorial 2D	Prof. Albert Wang , University of California
Session 3A	Photovoltaic Technology and Manufacturing
Session 3B	Electronic Design Automation
Session 3C	Micro Electro Mechanical System MEMS
Tutorial 3D	David Bergman, IPC
Session 4A	Test and Verification
Session 4B	PCB and PWB Technology and Manufacturing
Session 4C	IC Packaging Technology
Tutorial 4D	Dr. Rajiv V Joshi , IBM

A S Q E D 2010 Introduction

ASQED 2010 is the second event organized by the International Society for Quality Electronic Design in Asia. This event is being co-organized and managed by Malaysia Institute of Microsystems (MIMs) and Malaysian Industry Government Group for High Technology (MIGHT) with support from Malaysian Industrial Development Authority (MIDA). This symposium creates a platform for leading industrial and educational entity such as Intel Malaysia, Freescale Semiconductor, STATS ChipPAC Malaysia, Swinburne University of Technology and Monash University (Sunway Campus) as committee members. ASQED 2010 strives to bridge the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design and intends to highlight and accelerate co-operation among the IC design, EDA, Semiconductor Process Technology, IC Packaging, Test, and Manufacturing communities. ASQED 2010 spans over two days, with four parallel tracks, hosting near 100 technical presentations, several keynote speakers, tutorials and other informal meetings. Conference Proceedings will be published by IEEE and posted in the IEEE digital library.

Submission of Papers

Paper submission must be done on-line through the conference web site at www.isqed-asia.org. The guidelines for the final paper format are provided on the symposium web-site. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 10 pages) along with abstract of about 200 words. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. Please check the as-printed appearance of your paper before sending your paper. In case of any problems, email info2010@isqed-asia.org. Please note the following important dates:

Paper Submission Deadline	March 16, 2010
Acceptance Notification	April 24, 2010
Final Camera-Ready paper	June 2, 2010

Registration Information:

This Conference is registered under a special PSMB : SBL-KHAS Program and is HRDF Claimable (for Malaysian Companies).

Online Registration: www.isqed-asia.org (1 March 2010 onwards)

Conference Fee	RM 1,200
* Student	RM 600
* SHRDC, Committee & IEEE Members	RM 1,000
Conference + Tutorial Fees (Include Tutorial hand-out)	RM 1,500

All Fees are inclusive of two teas, lunch, program booklet

*Kindly provide Student ID and IEEE Membership ID for processing.
For group registration, please proceed to email or fax Registration Form (separate document) and Payment details to ASQED 2010 Secretariat.

2nd Asia Symposium on Quality Electronic Design
www.isqed-asia.org
ASQED 2010

The Secretariat
Malaysia Institute of Microsystems (MIMS)
c/o SHRDC (Selangor Human Resource Development Centre)
1A, 1st Floor, Block 2
Pusat Perniagaan Worldwide
Jalan Tinju 13/50, Section 13
40100 Shah Alam
Selangor D.E. , Malaysia

Tel: +60 3 55133 560
Fax: +60 3 55133 490
Email: info2010@isqed-asia.org

Office hours: Monday to Friday
9am to 5pm
GMT +8:00 (Malaysia)